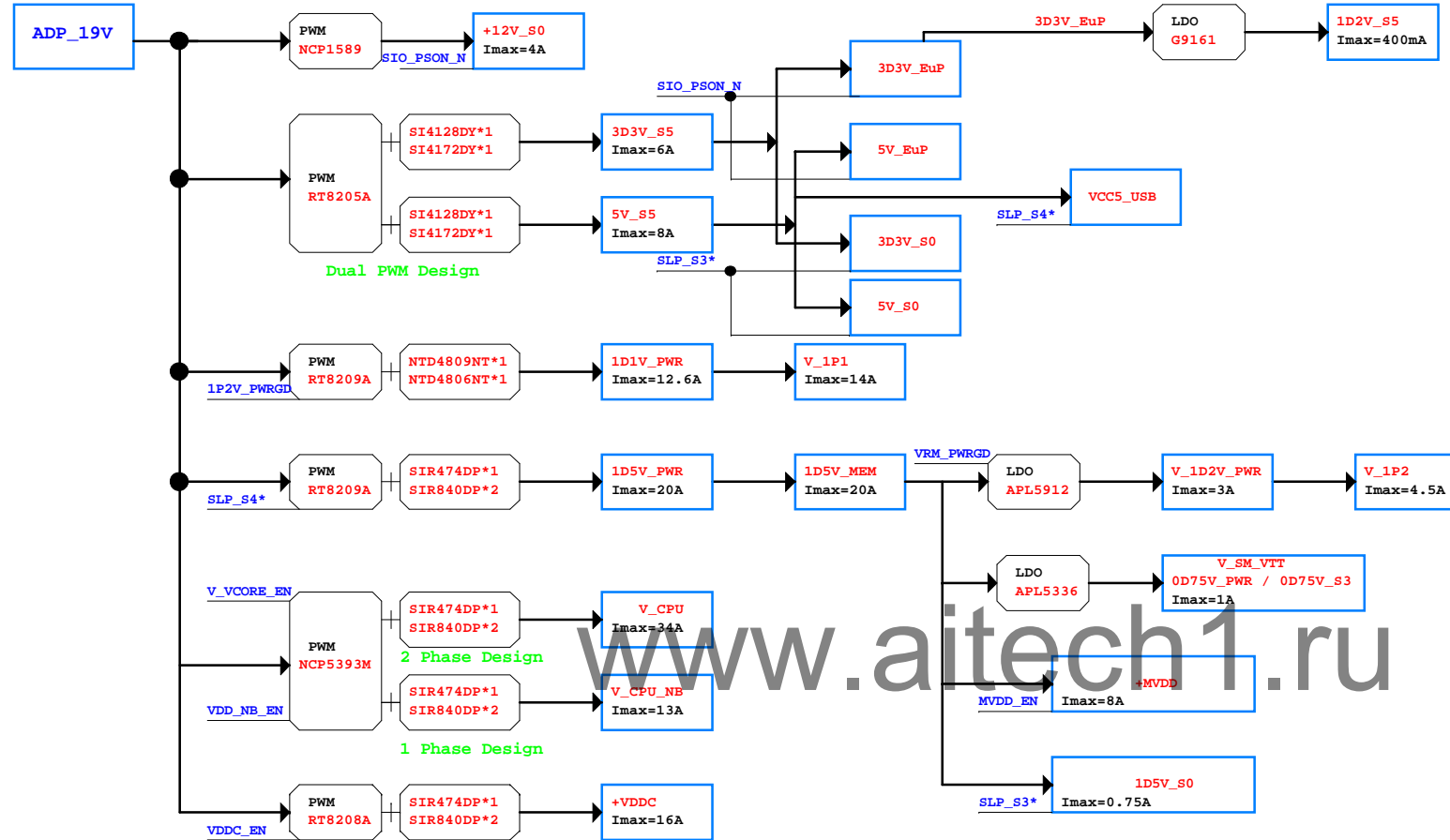


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Sheet 15	RS780L-HT LINK0 I/F	
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**PROJECT NAME: B305**  
**BOARD VERSION: 1B**  
**DATE: 202 mm X 230 mm**



DC\_IN



## CPU AM3(45W)

CPU VORE+CPU NB (0.8~1.55V 34A)	
VDDR 1.2V	1.4A
CPU VDDA 2.5V 110mA	
1.5V	1.75A
VDDIO 1.2V	1.4A

RS780L	
VDDHT/RX 1.1V	1.2A
VDDHTTX 1.2V	0.5A
VDDPCIE 1.1V	2A
NB CORE VDDC 1.1V 10A	
VDDA18PCIE 1.8V	0.9A
PLLs 1.8V	0.1A
VDD18/VDD18_MEM 1.8V	0.01A
VDD_MEM 1.8V/1.5V	0.5A
AVDD 3.3V	0.135A

SB710	
X4 PCIE 0.8A 1.2V(S0, S1)	
ATA IO	0.5A
ATA PLL	0.01A
PCIE PVDD 80mA	
SB CORE 0.6A	
CLOCK (S0, S1)	
1.2V S5 PW	0.22A
3.3V S5 PW	0.01A
USB CORE IO	0.2A
3.3V IO	0.45A

PCIE x2 Mini Card	
3D3V_S0	+3.3V 3A
+12V_S0	+12V 0.5A
1D5V_S0	+3.3VSB 0.375A

BIOS ROM(8Mb)	
3D3V_S0	+3.3V 67mA

CPU Fan	
+12V_S0	+12V_S0 0.5A
System Fan	
+12V_S0	+12V_S0 0.5A

SO-DIMM	
1D5V_MEM	DDR3 2GB V_SM +1.5V 3A
V_SM_VTT	V_SM_VTT +0.75V 1.2A

Clock Generator ICS9LPRS480AKLFT	
3D3V_S0	+3.3V 0.33A

RTL8103EL	
3D3V_S0	+3.3V 330mA

VT6325	
3D3V_S0	+3.3V 120mA

ITE 8758E	
3D3V_S0	+3.3V 120mA

RTD2280L	
3D3V_S0	+3.3V 385mA
VCC5_USB	
USB X2 Side	VCC5_USB 1.0A
USB X4 Rear	VCC5_USB 2.0A
USB X4 Device	VCC5_USB 2.5A

LDO APL5930	
3D3V_S0	1D8V(NB) Imax=1A

LDO APL5312	
3D3V_S0	2D5V Imax=200mA

LDO APL5930	
3D3V_S0	+1.8V_REG Imax=1.3A

LDO APL5912	
3D3V_S0	+1.0V_REG Imax=1.7A

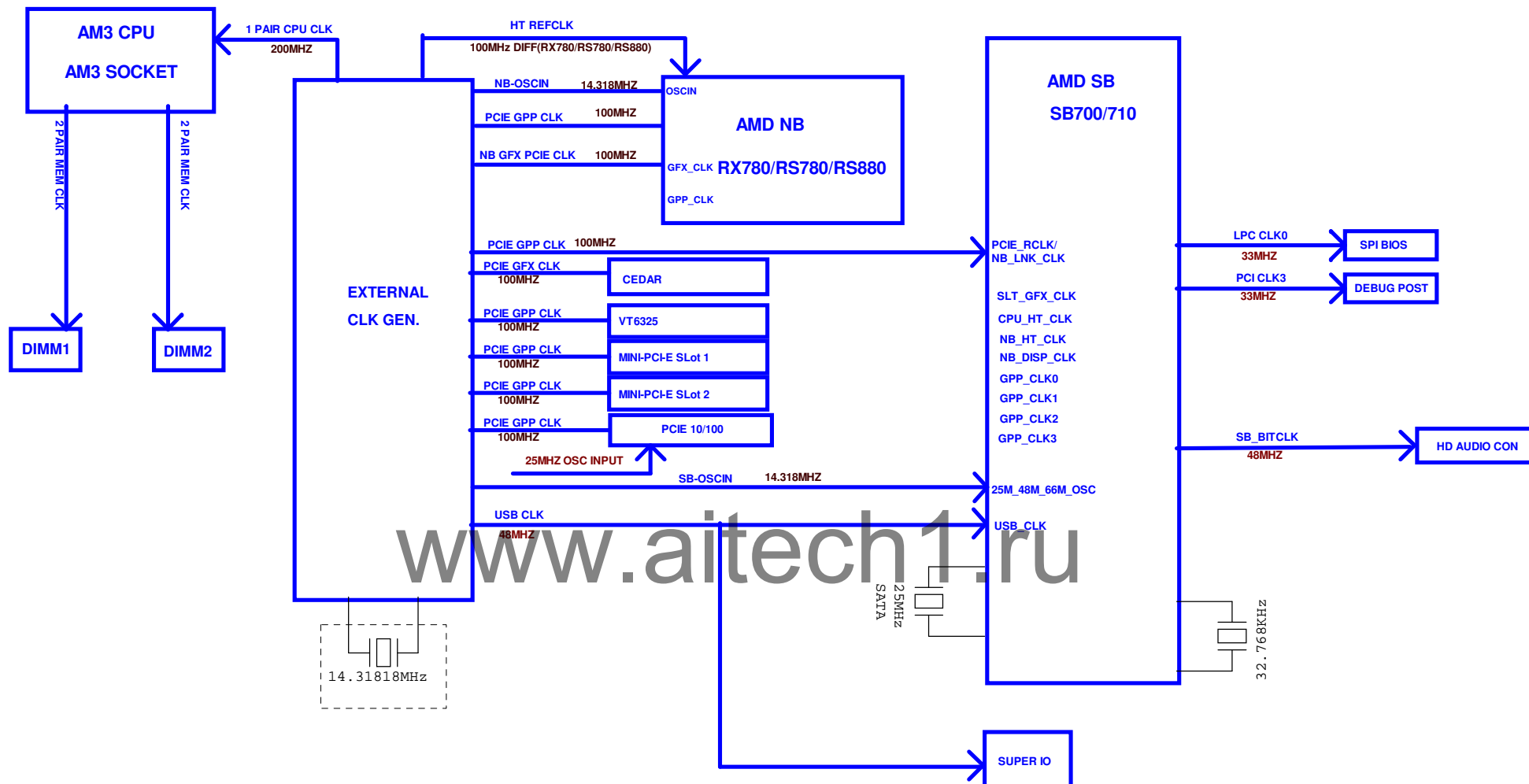
&lt;Variant Name&gt;

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Wistron Incorporated  
21F, 88, Hei Tai Wu Rd  
Hsichih, Taipei

## POWER DELIVERY CHART

Size C	Document Number	Rev
	Barbados	1B
Date:	Saturday, April 28, 2010	Sheet 2 of 62



<Variant Name>

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**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title

**CLOCK MAP**

Size  
Custom

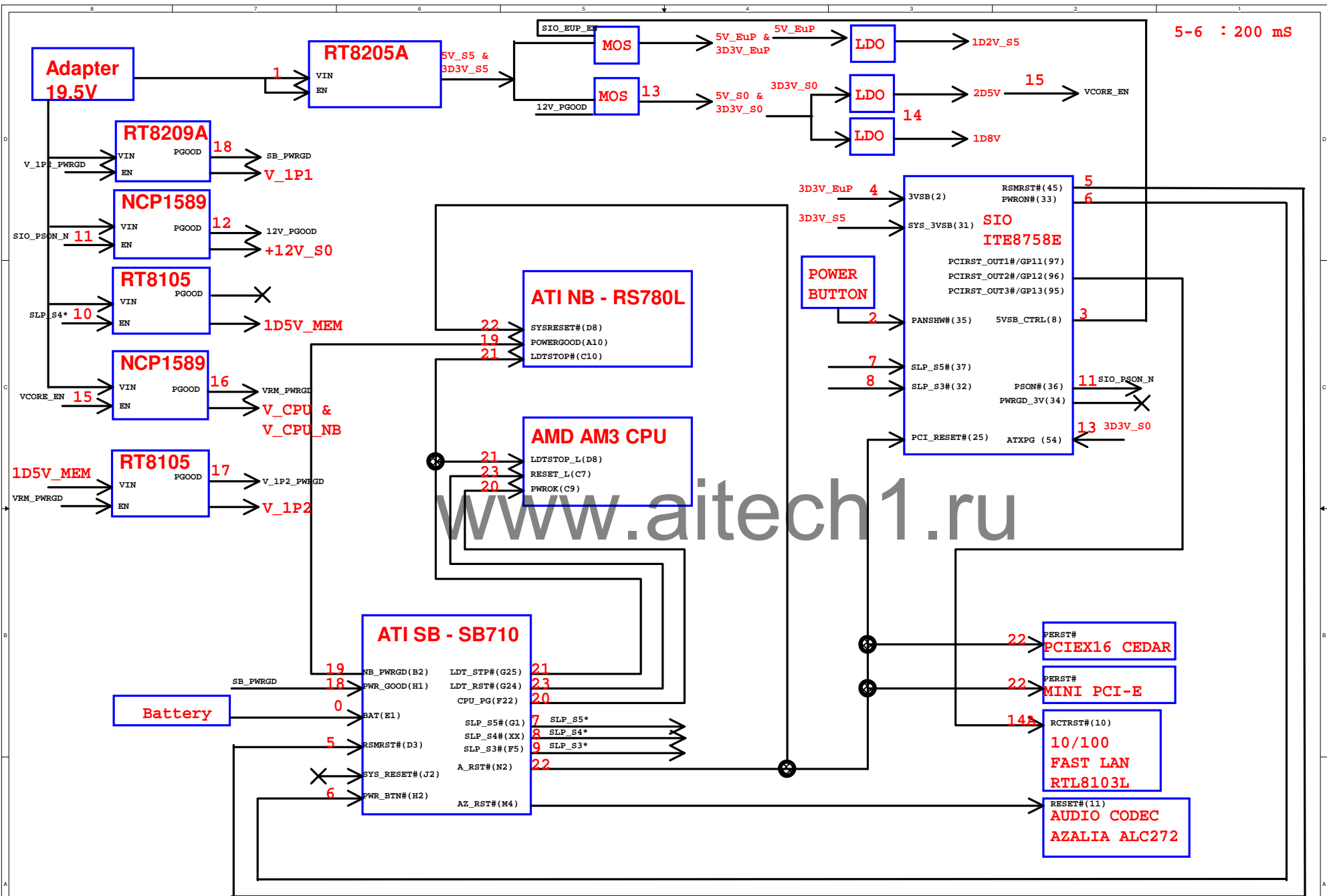
Document Number

**Barbados**

Rev  
1B

Date: Saturday, April 24, 2010

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# RESET/POWER GOOD MAP





## GPIO Table

PIN NAME	PIN#	POWER WELL	USAGE	Default Type	Default Value	Enable Setting	Notes
GPIO0	MAIN	NO USE		GPIO	Low		Integrated Pull-down 10K
GPIO2	MAIN	SB_SPKR	Native(Speaker)	GPIO	HIGH		PC BEEP (Integrated Pull-up 8.2K)
GPIO3	MAIN	NO USE		GPIO			
GPIO4	MAIN	NO USE		GPIO			
GPIO5	MAIN	NO USE		GPIO			
GPIO6	MAIN	NO USE		GPIO			
GPIO8	MAIN	NO USE		GPIO			
GPIO9	MAIN	NO USE		GPIO			
GPIO10	MAIN	NO USE		GPIO			
GPIO11	RESUME	SPI_DATAOUT	Native(SPI ROM Data Out)	GPIO	Low		SPI Integrated Pull-down 10K
GPIO12	RESUME	SPI_DATAIN	Native(SPI ROM Data In)	GPIO	Low		SPI Integrated Pull-down 10K
GPIO13	MAIN	SPI_WMM	GPD (Low)	GPD	Low		SPI Write Protect
GPIO14	RESUME	NO USE		GPD	Low		
GPIO15	MAIN	TV_EN		GPD	HIGH		
GPIO16	MAIN	WIRELESS_EN		GPD	HIGH		
GPIO17	MAIN	WIRELESS_EN		GPD	HIGH		
GPIO18	MAIN	AUTO_COLOR_SEL		GPD	HIGH		
GPIO19	MAIN	UNUSUS		GPD	HIGH		
GPIO20	MAIN	NO USE		GPD	HIGH		
GPIO21	MAIN	NO USE		GPD	HIGH		
GPIO22	MAIN	NO USE		GPD	HIGH		
GPIO23	MAIN	NO USE		GPD	HIGH		
GPIO24	MAIN	NO USE		GPD	HIGH		
GPIO25	MAIN	NO USE		GPD	HIGH		
GPIO26	MAIN	NO USE		GPD	HIGH		
GPIO27	MAIN	NO USE		GPD	HIGH		
GPIO28	MAIN	NO USE		GPD	HIGH		
GPIO29	MAIN	NO USE		GPD	HIGH		
GPIO30	MAIN	NO USE		GPD	HIGH		
GPIO31	RESUME	SPI_HOST	Native(SPI ROM Chip Select 1)	GPIO			Integrated Pull-up 10K
GPIO32	RESUME	SPI_CS#	Native(SPI ROM Chip Select 1)	GPIO			Integrated Pull-up 10K
GPIO33	MAIN	WIRELESS_EN		GPIO			Integrated Pull-up 8.2K
GPIO34	MAIN	NO USE		GPIO			Integrated Pull-up 8.2K
GPIO35	MAIN	NO USE		GPIO			Integrated Pull-up 8.2K
GPIO36	MAIN	NO USE		GPIO			Integrated Pull-up 8.2K
GPIO37	MAIN	NO USE		GPIO			Integrated Pull-up 8.2K
GPIO38	MAIN	NO USE		GPIO			Integrated Pull-down 10K
GPIO39	MAIN	NO USE		GPIO			Integrated Pull-down 10K
GPIO40	MAIN	NO USE		GPIO			Integrated Pull-down 10K
GPIO41	MAIN	NO USE		GPIO			Integrated Pull-down 10K
GPIO42	RESUME	NO USE		GPIO			Integrated Pull-down 50K
GPIO43	RESUME	AC2_DOWN	Native(HD Audio Serial Data In 1)	GPIO			Integrated Pull-down 50K
GPIO44	RESUME	NO USE		GPIO			Integrated Pull-down 50K
GPIO45	RESUME	NO USE		GPIO			Integrated Pull-down 50K
GPIO46	RESUME	NO USE		GPIO			Integrated Pull-down 50K
GPIO47	RESUME	SPI_CLK	Native(SPI ROM Clock)	GPIO			Integrated Pull-down 10K
GPIO48	MAIN	NO USE		GPIO			Integrated Pull-up 8.2K
GPIO49	MAIN	NO USE		GPIO			Integrated Pull-up 8.2K
GPIO50	MAIN	BOARD_ID	HIGH: MXM / Low: UMA	GPIO			
GPIO51	MAIN	NO USE		GPIO			
GPIO52	MAIN	NO USE		GPIO			
GPIO53	RESUME	NO USE		GPIO			
GPIO54	RESUME	NO USE		GPIO			
GPIO55	RESUME	NO USE		GPIO			
GPIO56	RESUME	NO USE		GPIO			
GPIO57	RESUME	NO USE		GPIO			
GPIO58	RESUME	NO USE		GPIO			
GPIO59	RESUME	NO USE		GPIO			
GPIO60	RESUME	NO USE		GPIO			
GPIO61	RESUME	NO USE		GPIO			
GPIO62	RESUME	NO USE		GPIO			
GPIO63	RESUME	NO USE		GPIO			
GPIO64	RESUME	TEMP_ALERT	Native(Temperature Alert)	GPIO			
GPIO65	MAIN	IS_DISABLE	Native(Bus Master Request)	GPIO			
GPIO66	RESUME	NO USE		GPIO			Integrated Pull-up 10K
GPIO67	MAIN	ICH_SATA_LED	Native(Serial ATA Activity)	GPIO			OD
GPIO68	MAIN	LDOWM_SB	Native(LPC DMA Req 1)	GPIO			Integrated Pull-up 15K
GPIO69	MAIN	FP_DETECT		GPIO			Integrated Pull-up 15K
GPIO70	MAIN	NO USE		GPIO			Integrated Pull-up 15K
GPIO71	MAIN	NO USE		GPIO			
GPIO72	MAIN	NO USE		GPIO			
GPIO73	MAIN	NO USE		GPIO			

Board ID	GPIO50
MXM	1
UMA	0

## SB700 GPIO/O

PIN NAME	PIN#	POWER WELL	USAGE	Type	Default Type	Enable Setting	NOTES
USB_OC0# / GPM0#		RESUME	OC'01	GPIO	VCC3_35B	LOW	
USB_OC1# / GPM1#		RESUME	OC'01	GPIO	VCC3_35B	LOW	
USB_OC2# / GPM2#		RESUME	OC'23	GPIO	VCC3_35B	LOW	
USB_OC3# / GPM3#		RESUME	OC'23	GPIO	VCC3_35B	LOW	
USB_OC4# / GPM4#		RESUME	OC'45	GPIO	VCC3_35B	LOW	
USB_OC5# / DDR3_RST# / GPM5#		RESUME	OC'45	GPIO	VCC3_35B	LOW	
USB_OC6# / GEVENT6#		RESUME	OC'6	GPIO	VCC3_35B	LOW	
USB_OC7# / GEVENT7#		RESUME	NO USE	GPIO	VCC3_35B	LOW	
USB_OC8# / AZ_DOCK_RST# / GPM8#		RESUME	NO USE	GPIO	VCC3_35B	High	
USB_OC9# / SLP_S2# / GPM9#		RESUME	NO USE	GPIO	VCC3_35B		
EXTEVENT0#		RESUME	A20GATE	GPIO	VCC3_35B		
EXTEVENT1#		MAIN	KBRST*	GPIO	VCC3_35B		
GEVENT2#		RESUME	CPU_THERMTRIP	GPIO	VCC3_35B		
GEVENT3#		RESUME	LPC_PME*	GPIO	VCC3_35B		
GEVENT4#		RESUME	NO USE	GPIO	VCC3_35B		
GEVENT5#		RESUME	S3_STATE	GPIO	VCC3_35B		
BLINK# / GPM6#		RESUME	NO USE	GPIO	VCC3_35B	LOW	GPM
GPM7#		RESUME	FP_RESET*	GPIO	VCC3_35B		
GEVENT8#		RESUME	WOL	GPIO	VCC3_35B		
SDA0 / GPOC0#		MAIN	SMBCLK	GPIO	VCC3_35B		
SDA0 / GPOC1#		MAIN	SMBDATA	GPIO	VCC3_35B		
SDA1 / GPOC2#		RESUME	ALERT_CLK	GPIO	VCC3_35B		
SDA1 / GPOC3#		RESUME	ALERT_DATA	GPIO	VCC3_35B		
IMS_GPIO13	E20		CPU_SIC				
IMS_GPIO14	E21		CPU_SID				
IMS_GPIO16	D19		IMC_GPIO16				
IMS_GPIO17	E18		IMC_GPIO17				

SOURCE	SIGNAL NAME	LINKED DEVICES
NB	DACSCL0/DACSDA0	
	DACSCL1/DACSDA1	
SB	SCLK0/SDATA0	
	SCLK1/SDATA1	

SUPER I/O: ITE 8758E

# CPU FAN

41 CPU\_FAN\_CTRL CPU\_FAN\_CTRL  
41 CPU\_FAN\_TACH CPU\_FAN\_TACH

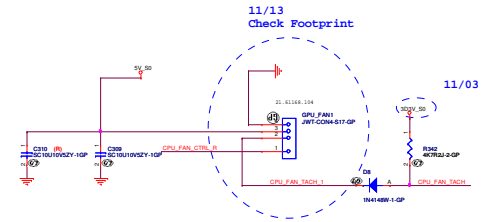
# SYSTEM FAN

41 REAR\_FAN\_CTRL REAR\_FAN\_CTRL  
41 REAR\_FAN\_TACH REAR\_FAN\_TACH

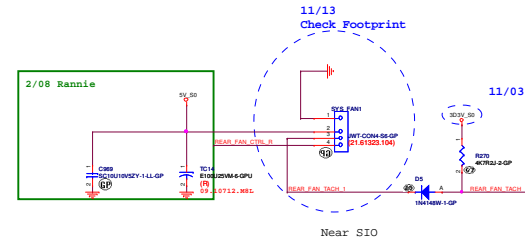
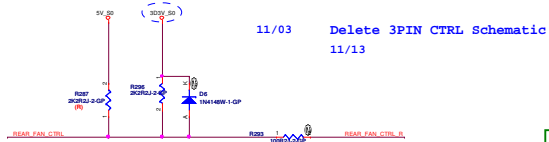
## ONLY FOR 4 PIN FAN CONTROL



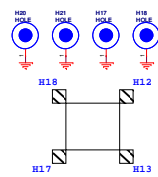
11/06



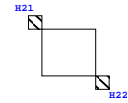
## 2nd FAN



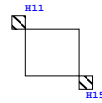
## CPU MOUNTING HOLE-PTH



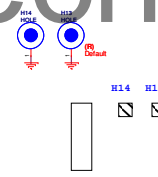
## GPU MOUNTING HOLE-NPTH



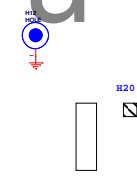
## SB MOUNTING HOLE-PTH



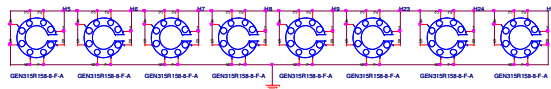
## MINI PCIE 1 MOUNTING HOLE-PTH



## MINI PCIE 1 MOUNTING HOLE-PTH



## PCB MOUNTING HOLES-PTH



## CPU CLK

10 CPUCLK CPUCLK#

## PCIEx16 CLK

54 PCIe\_REFCLKP PCIe\_REFCLKN

## LAN CLK

39 KG\_GFX\_CLKP KG\_GFX\_CLKN

## NB HCLK

17 KG\_NBHT\_CLKP KG\_NBHT\_CLKN

## NB Ref CLK

17 KG\_NBREF\_CLKP KG\_NBREF\_CLKN

## NB GFX CLK

17 KG\_NBGFCLKP KG\_NBGFCLKN

To SB

## Mini PCI-E CLK 1103 Modify

35 CLK\_PCE\_MINI# CLK\_PCE\_MINI#  
30 CLK\_PCE\_MINI# CLK\_PCE\_MINI#  
30 CLK\_PCE\_MINI# CLK\_PCE\_MINI#  
30 CLK\_PCE\_MINI# CLK\_PCE\_MINI#  
35 CLK\_PCE\_OR\_P CLK\_PCE\_OR\_P  
35 CLK\_PCE\_OR\_N CLK\_PCE\_OR\_N  
35 MIN2\_CLKREQ# MIN2\_CLKREQ#  
30 MIN2\_CLKREQ# MIN2\_CLKREQ#

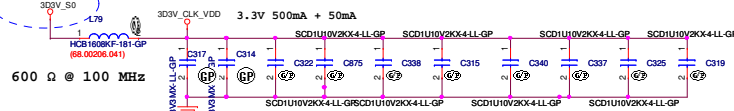
21,24,28,30,41,55 SMBCLK SMBDATA

41 SIO\_CLK48 KG\_CLK\_48M\_USB

17 OSC\_14M\_NB CLK14\_SB

47,49 1P2V\_PWRGD 1P2V\_PWRGD

11/04



11/04

11/11

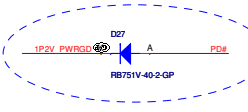
May use one 22uF instead?

## NB CLOCK INPUT TABLE

NB CLOCKS	RS780
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	1.4M SE (1.1V)
REFCLK_N	val
GFX_REFCLKP	100M DIFF
GPP_REFCLK	100M DIFF(OUT)
GPPSB_REFCLK	100M DIFF

\* the GFX\_REFCLK input is required for all cases

11/03 Modify



11/09

SEL_SATA	1	100 Mhz non-spreading differential SRC clock
REF1	0*	100 Mhz spreading differential SRC clock
SEL_HIT66	1	86 Mhz 3.3V single ended HTT clock
REF0	0*	100 Mhz differential HTT clock

\* default

11/04



Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

For NB GFX

For PCIEx16

11/03 CLKREQ# Internal pull high

11/14

11/04

SCH5147 3.3V

1107 Delete 14M for SIO

3/01 Rannie

OSC 14M NB  
RS780 1.1V 158R/90.9R

&lt;Variant Name&gt;

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21F, 88, Hei Tai Wu Rd  
Hsichih, Taipei

EXTERNAL CLOCK GENERATOR

Barbados

Date: Saturday, April 24, 2010 Sheet 8 of 62

# HT Interface

15 HT\_CLKIN1\_P << HT\_CLKIN1\_P  
 15 HT\_CLKIN1\_N << HT\_CLKIN1\_N  
 15 HT\_CLKIN0\_P << HT\_CLKIN0\_P  
 15 HT\_CLKIN0\_N << HT\_CLKIN0\_N

15 HT\_CTLIN1\_P << HT\_CTLIN1\_P  
 15 HT\_CTLIN1\_N << HT\_CTLIN1\_N  
 15 HT\_CTLIN0\_P << HT\_CTLIN0\_P  
 15 HT\_CTLIN0\_N << HT\_CTLIN0\_N

15 HT\_CLKOUT1\_P << HT\_CLKOUT1\_P  
 15 HT\_CLKOUT1\_N << HT\_CLKOUT1\_N  
 15 HT\_CLKOUT0\_P << HT\_CLKOUT0\_P  
 15 HT\_CLKOUT0\_N << HT\_CLKOUT0\_N

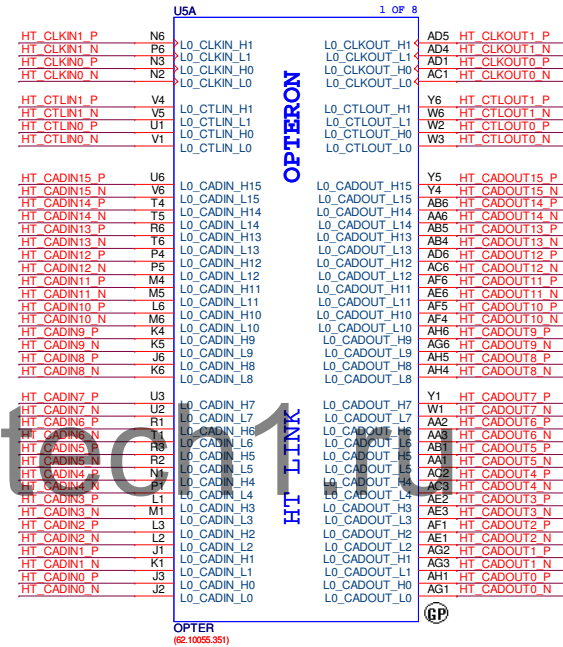
15 HT\_CTLOUT1\_P << HT\_CTLOUT1\_P  
 15 HT\_CTLOUT1\_N << HT\_CTLOUT1\_N  
 15 HT\_CTLOUT0\_P << HT\_CTLOUT0\_P  
 15 HT\_CTLOUT0\_N << HT\_CTLOUT0\_N

15 HT\_CADIN7\_P << HT\_CADIN7\_P  
 15 HT\_CADIN7\_N << HT\_CADIN7\_N  
 15 HT\_CADIN6\_P << HT\_CADIN6\_P  
 15 HT\_CADIN6\_N << HT\_CADIN6\_N  
 15 HT\_CADIN5\_P << HT\_CADIN5\_P  
 15 HT\_CADIN5\_N << HT\_CADIN5\_N  
 15 HT\_CADIN4\_P << HT\_CADIN4\_P  
 15 HT\_CADIN4\_N << HT\_CADIN4\_N  
 15 HT\_CADIN3\_P << HT\_CADIN3\_P  
 15 HT\_CADIN3\_N << HT\_CADIN3\_N  
 15 HT\_CADIN2\_P << HT\_CADIN2\_P  
 15 HT\_CADIN2\_N << HT\_CADIN2\_N  
 15 HT\_CADIN1\_P << HT\_CADIN1\_P  
 15 HT\_CADIN1\_N << HT\_CADIN1\_N  
 15 HT\_CADIN0\_P << HT\_CADIN0\_P  
 15 HT\_CADIN0\_N << HT\_CADIN0\_N

15 HT\_CADIN15\_P << HT\_CADIN15\_P  
 15 HT\_CADIN15\_N << HT\_CADIN15\_N  
 15 HT\_CADIN14\_P << HT\_CADIN14\_P  
 15 HT\_CADIN14\_N << HT\_CADIN14\_N  
 15 HT\_CADIN13\_P << HT\_CADIN13\_P  
 15 HT\_CADIN13\_N << HT\_CADIN13\_N  
 15 HT\_CADIN12\_P << HT\_CADIN12\_P  
 15 HT\_CADIN12\_N << HT\_CADIN12\_N  
 15 HT\_CADIN11\_P << HT\_CADIN11\_P  
 15 HT\_CADIN11\_N << HT\_CADIN11\_N  
 15 HT\_CADIN10\_P << HT\_CADIN10\_P  
 15 HT\_CADIN10\_N << HT\_CADIN10\_N  
 15 HT\_CADIN9\_P << HT\_CADIN9\_P  
 15 HT\_CADIN9\_N << HT\_CADIN9\_N  
 15 HT\_CADIN8\_P << HT\_CADIN8\_P  
 15 HT\_CADIN8\_N << HT\_CADIN8\_N

15 HT\_CADOUT7\_P << HT\_CADOUT7\_P  
 15 HT\_CADOUT7\_N << HT\_CADOUT7\_N  
 15 HT\_CADOUT6\_P << HT\_CADOUT6\_P  
 15 HT\_CADOUT6\_N << HT\_CADOUT6\_N  
 15 HT\_CADOUT5\_P << HT\_CADOUT5\_P  
 15 HT\_CADOUT5\_N << HT\_CADOUT5\_N  
 15 HT\_CADOUT4\_P << HT\_CADOUT4\_P  
 15 HT\_CADOUT4\_N << HT\_CADOUT4\_N  
 15 HT\_CADOUT3\_P << HT\_CADOUT3\_P  
 15 HT\_CADOUT3\_N << HT\_CADOUT3\_N  
 15 HT\_CADOUT2\_P << HT\_CADOUT2\_P  
 15 HT\_CADOUT2\_N << HT\_CADOUT2\_N  
 15 HT\_CADOUT1\_P << HT\_CADOUT1\_P  
 15 HT\_CADOUT1\_N << HT\_CADOUT1\_N  
 15 HT\_CADOUT0\_P << HT\_CADOUT0\_P  
 15 HT\_CADOUT0\_N << HT\_CADOUT0\_N

15 HT\_CADOUT15\_P << HT\_CADOUT15\_P  
 15 HT\_CADOUT15\_N << HT\_CADOUT15\_N  
 15 HT\_CADOUT14\_P << HT\_CADOUT14\_P  
 15 HT\_CADOUT14\_N << HT\_CADOUT14\_N  
 15 HT\_CADOUT13\_P << HT\_CADOUT13\_P  
 15 HT\_CADOUT13\_N << HT\_CADOUT13\_N  
 15 HT\_CADOUT12\_P << HT\_CADOUT12\_P  
 15 HT\_CADOUT12\_N << HT\_CADOUT12\_N  
 15 HT\_CADOUT11\_P << HT\_CADOUT11\_P  
 15 HT\_CADOUT11\_N << HT\_CADOUT11\_N  
 15 HT\_CADOUT10\_P << HT\_CADOUT10\_P  
 15 HT\_CADOUT10\_N << HT\_CADOUT10\_N  
 15 HT\_CADOUT9\_P << HT\_CADOUT9\_P  
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 15 HT\_CADOUT8\_N << HT\_CADOUT8\_N

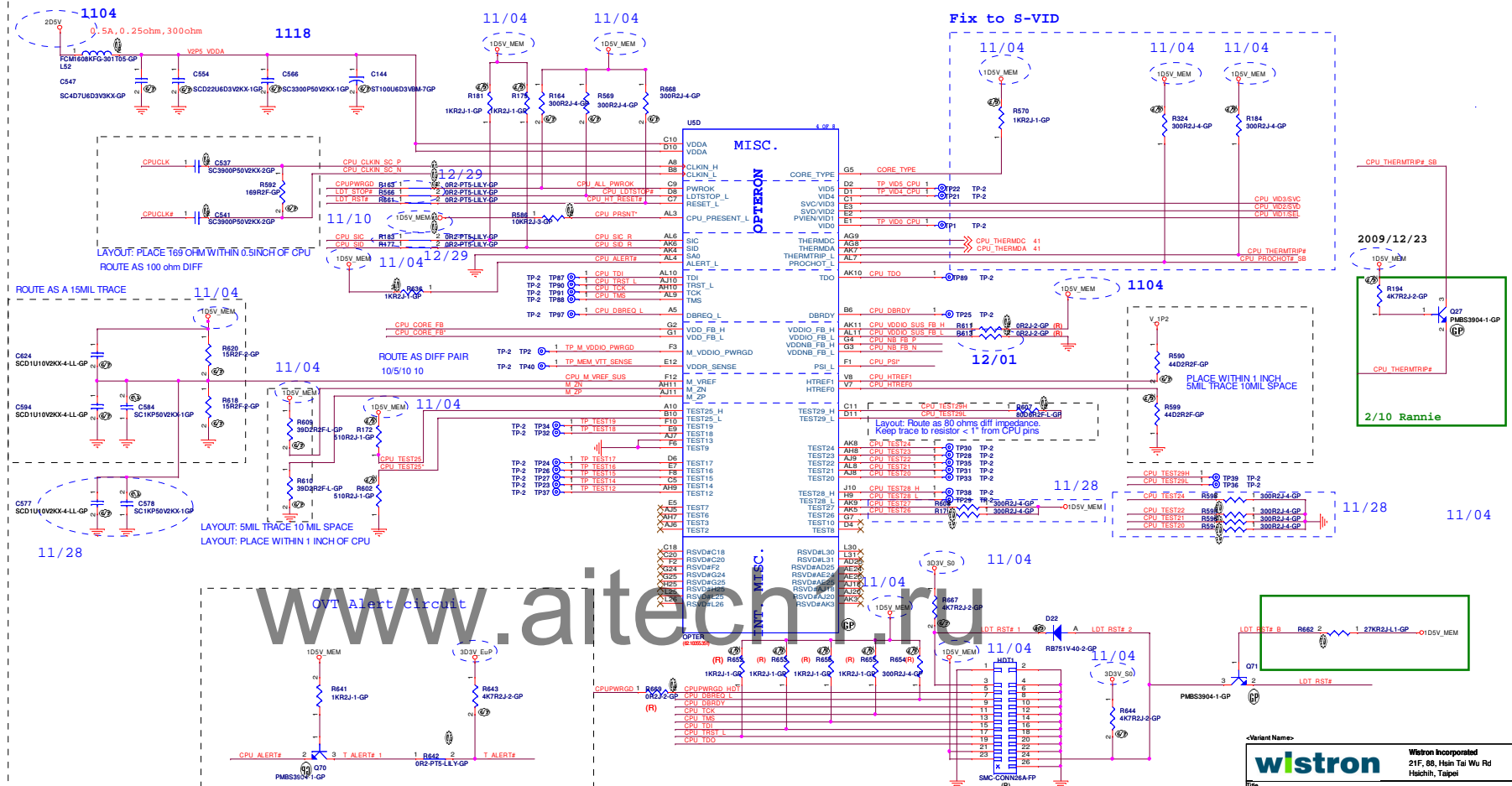


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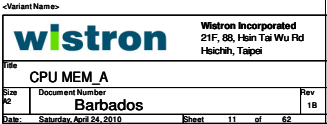
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<b>wistron</b>		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title <b>CPU HT Interface</b>			
Size A3	Document Number <b>Barbados</b>		Rev 1B
Date: Saturday, April 24, 2010	Sheet 9	of 62	

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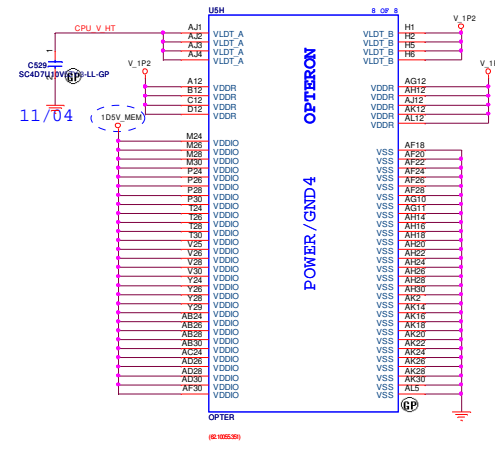
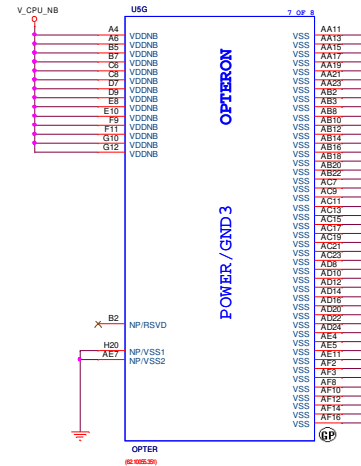
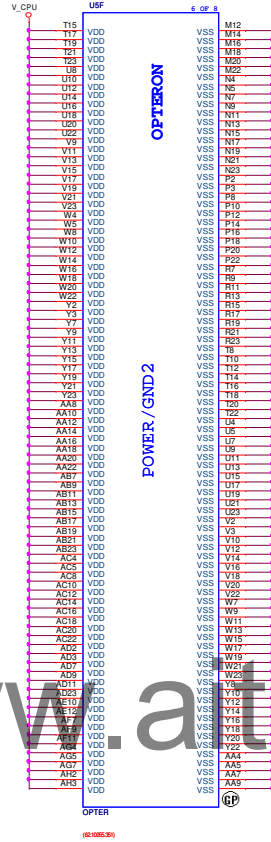
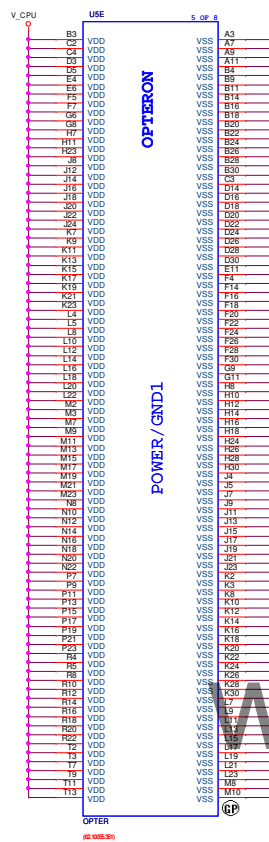
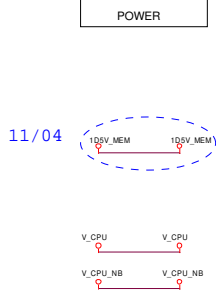
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Title CPU CNTL/STRAPS			
Size Custom	Document Number <b>Barbados</b>	Rev 1B	
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9 HT\_CADOUT0\_P >>> HT\_RXCAD0\_P  
9 HT\_CADOUT0\_N >>> HT\_RXCAD0\_N  
9 HT\_CADOUT1\_P >>> HT\_RXCAD1\_P  
9 HT\_CADOUT1\_N >>> HT\_RXCAD1\_N  
9 HT\_CADOUT2\_P >>> HT\_RXCAD2\_P  
9 HT\_CADOUT2\_N >>> HT\_RXCAD2\_N  
9 HT\_CADOUT3\_P >>> HT\_RXCAD3\_P  
9 HT\_CADOUT3\_N >>> HT\_RXCAD3\_N  
9 HT\_CADOUT4\_P >>> HT\_RXCAD4\_P  
9 HT\_CADOUT4\_N >>> HT\_RXCAD4\_N  
9 HT\_CADOUT5\_P >>> HT\_RXCAD5\_P  
9 HT\_CADOUT5\_N >>> HT\_RXCAD5\_N  
9 HT\_CADOUT6\_P >>> HT\_RXCAD6\_P  
9 HT\_CADOUT6\_N >>> HT\_RXCAD6\_N  
9 HT\_CADOUT7\_P >>> HT\_RXCAD7\_P  
9 HT\_CADOUT7\_N >>> HT\_RXCAD7\_N

9 HT\_CADOUT8\_P >>> HT\_RXCAD8\_P  
9 HT\_CADOUT8\_N >>> HT\_RXCAD8\_N  
9 HT\_CADOUT9\_P >>> HT\_RXCAD9\_P  
9 HT\_CADOUT9\_N >>> HT\_RXCAD9\_N  
9 HT\_CADOUT10\_P >>> HT\_RXCAD10\_P  
9 HT\_CADOUT10\_N >>> HT\_RXCAD10\_N  
9 HT\_CADOUT11\_P >>> HT\_RXCAD11\_P  
9 HT\_CADOUT11\_N >>> HT\_RXCAD11\_N  
9 HT\_CADOUT12\_P >>> HT\_RXCAD12\_P  
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9 HT\_CADOUT13\_P >>> HT\_RXCAD13\_P  
9 HT\_CADOUT13\_N >>> HT\_RXCAD13\_N  
9 HT\_CADOUT14\_P >>> HT\_RXCAD14\_P  
9 HT\_CADOUT14\_N >>> HT\_RXCAD14\_N  
9 HT\_CADOUT15\_P >>> HT\_RXCAD15\_P  
9 HT\_CADOUT15\_N >>> HT\_RXCAD15\_N

9 HT\_CLKOUT0\_P >>> HT\_RXCLK0\_P  
9 HT\_CLKOUT0\_N >>> HT\_RXCLK0\_N  
9 HT\_CLKOUT1\_P >>> HT\_RXCLK1\_P  
9 HT\_CLKOUT1\_N >>> HT\_RXCLK1\_N

9 HT\_CTLOUT0\_P >>> HT\_RXCTL0\_P  
9 HT\_CTLOUT0\_N >>> HT\_RXCTL0\_N  
9 HT\_CTLOUT1\_P >>> HT\_RXCTL1\_P  
9 HT\_CTLOUT1\_N >>> HT\_RXCTL1\_N

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HT\_TXCAD0\_N >>> HT\_CADIN0\_N 9  
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HT\_TXCAD1\_N >>> HT\_CADIN1\_N 9  
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HT\_TXCAD2\_N >>> HT\_CADIN2\_N 9  
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HT\_TXCAD3\_N >>> HT\_CADIN3\_N 9  
HT\_TXCAD4\_P >>> HT\_CADIN4\_P 9  
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HT\_TXCAD8\_P >>> HT\_CADIN8\_P 9  
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HT\_TXCLK1\_N >>> HT\_CLKIN1\_N 9

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HT\_TXCTL1\_N >>> HT\_CTLIN1\_N 9

USA				1 OF 6			
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HT_RXCAD1_N	Y23	HT_RXCAD1N	E25	HT_TXCAD1_N	E25	HT_TXCAD1_N	
HT_RXCAD2_P	V25	HT_RXCAD2P	F24	HT_TXCAD2_P	F24	HT_TXCAD2_P	
HT_RXCAD2_N	V24	HT_RXCAD2N	F25	HT_TXCAD2_N	F25	HT_TXCAD2_N	
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HT_RXCAD4_P	T25	HT_RXCAD4P	H23	HT_TXCAD4_P	H23	HT_TXCAD4_P	
HT_RXCAD4_N	T24	HT_RXCAD4N	H22	HT_TXCAD4_N	H22	HT_TXCAD4_N	
HT_RXCAD5_P	P22	HT_RXCAD5P	J25	HT_TXCAD5_P	J25	HT_TXCAD5_P	
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HT_RXCAD6_P	P25	HT_RXCAD6P	K24	HT_TXCAD6_P	K24	HT_TXCAD6_P	
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HT_RXCLK1_N	AA22	HT_RXCLK1N	L20	HT_TXCLK1_N	L20	HT_TXCLK1_N	
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HT_RXCALN	A24	HT_RXCALN	B25	HT_TXCALN	B25	HT_TXCALN	

Place < 100 mils  
from C23 and A24

(71.RS780.M15)

Place < 100 mils  
from B24 and B25

RS780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RS780	RS780
HT_RXCALP	49.9R (GND)	121K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP	100R	121K	301R
HT_TXCALN			

<Variant Name>

**wlstron**

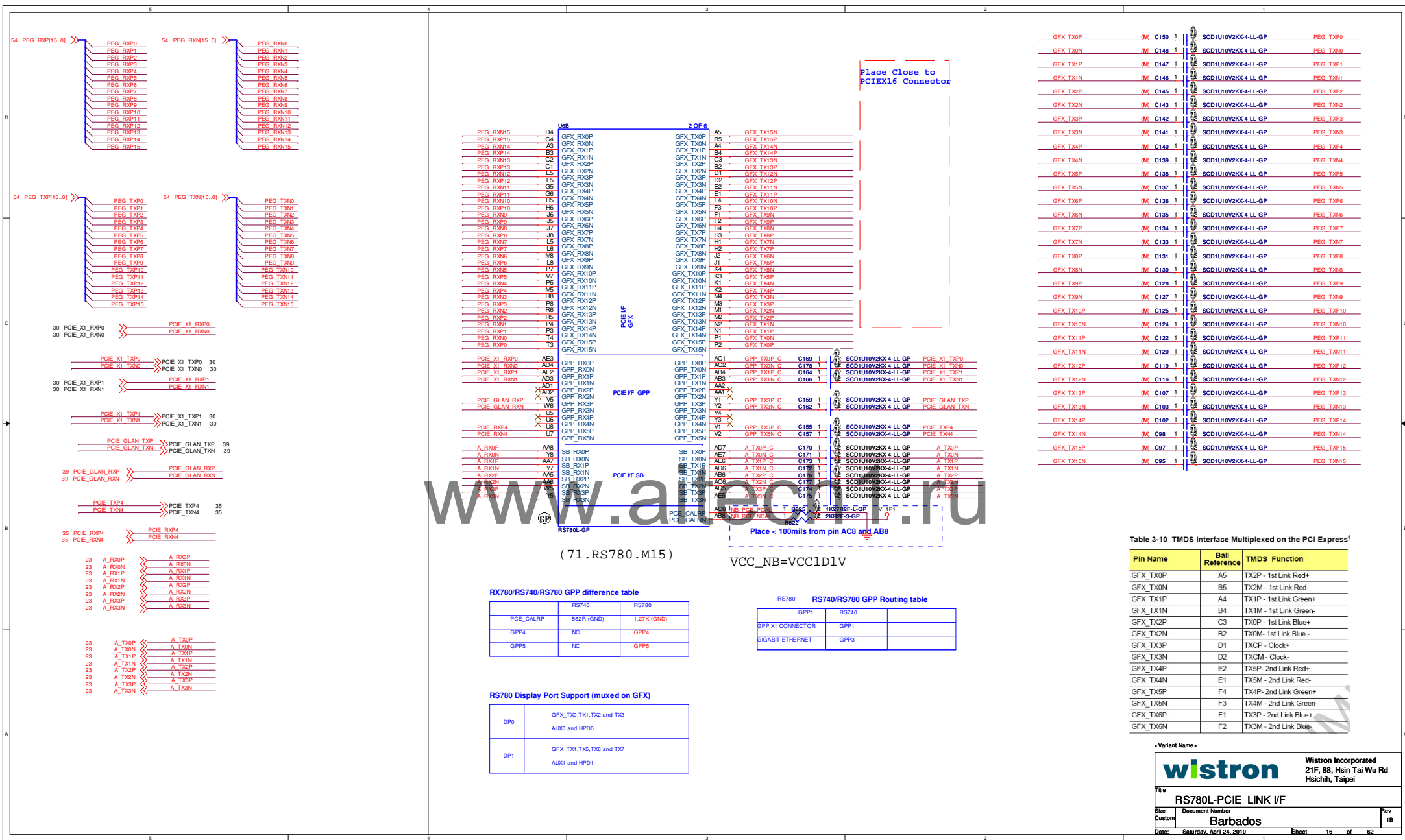
Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

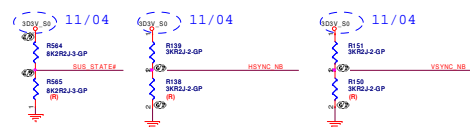
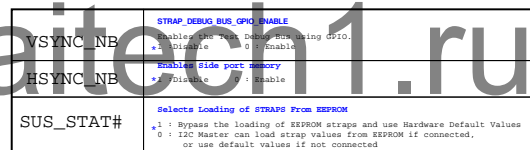
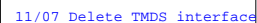
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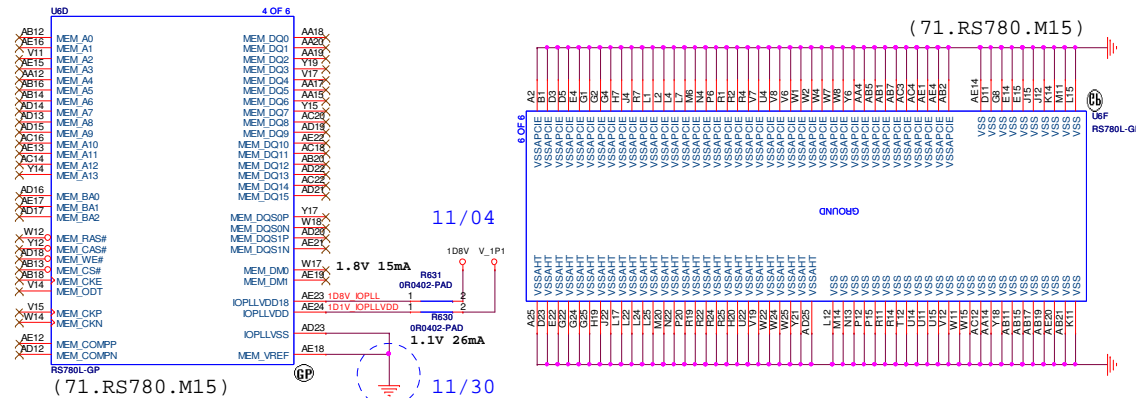
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Barbados

Rev  
1B

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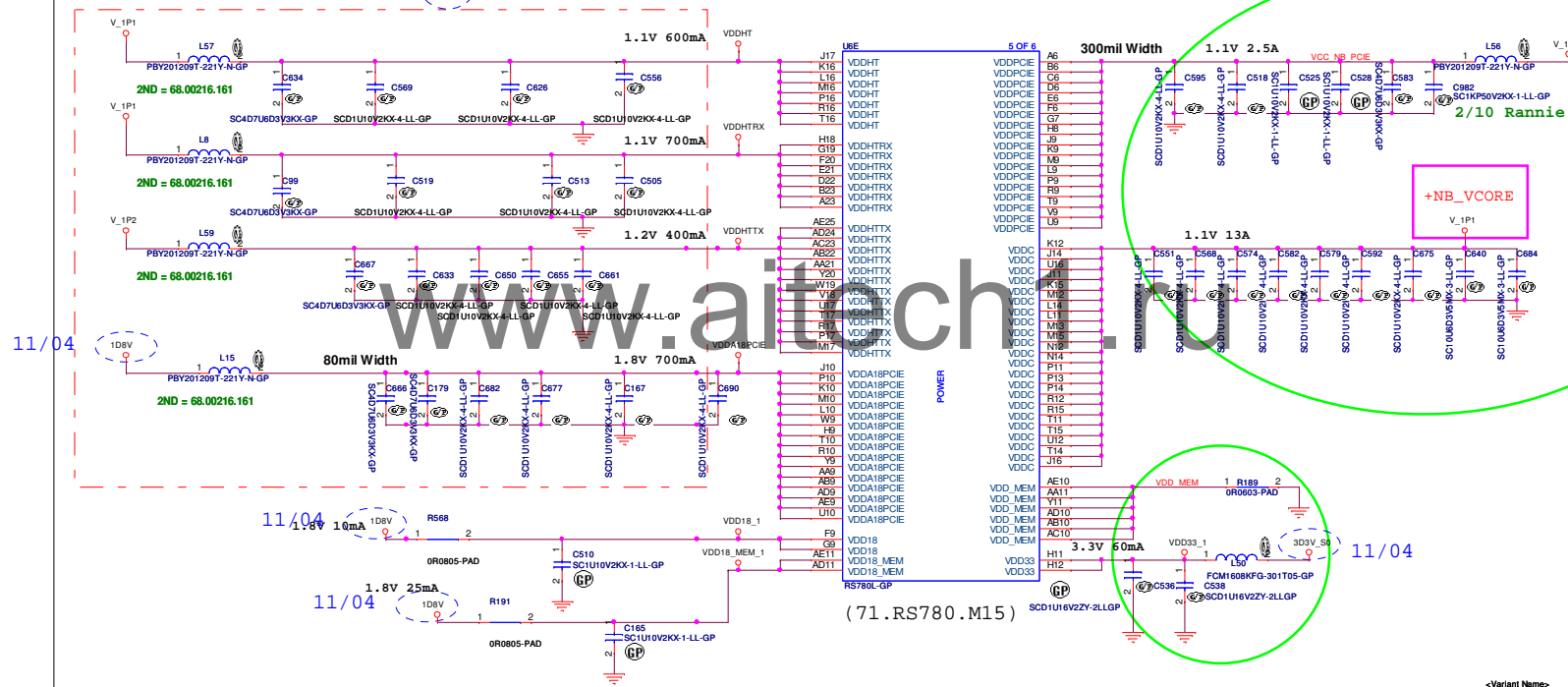






RS740/RX780/RS780 POWER DIFFERENCE TABLE


Pin Name	RS740	RX780	RS780	Pin Name	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDD	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	VDD18HTPLL	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDPC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLT18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC



5					4					3					2					1				
D																								
C																								
B																								
A																								


RESERVED

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<Variant Name>									
<div><div></div><div><b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei</div></div>									
Title RS760 (RESERVED)									
Size A		Document Number Barbados						Rev 1B	
Date:		Saturday, April 24, 2010				Sheet		19 of 62	

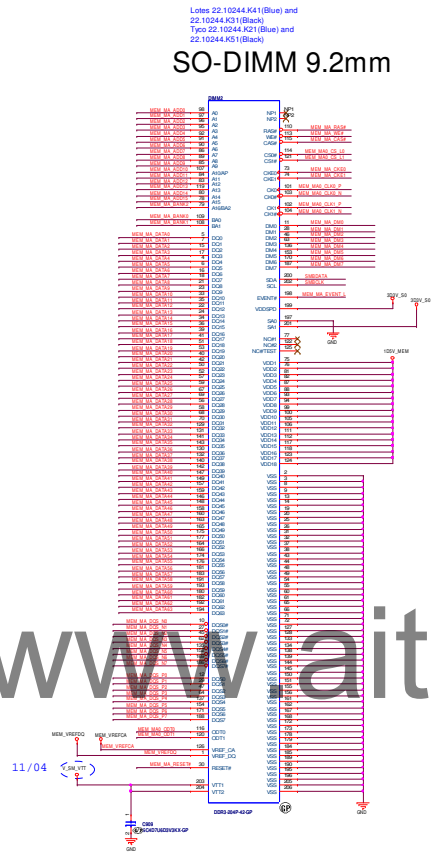
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C				C
B				B
A				A
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<Variant Name>

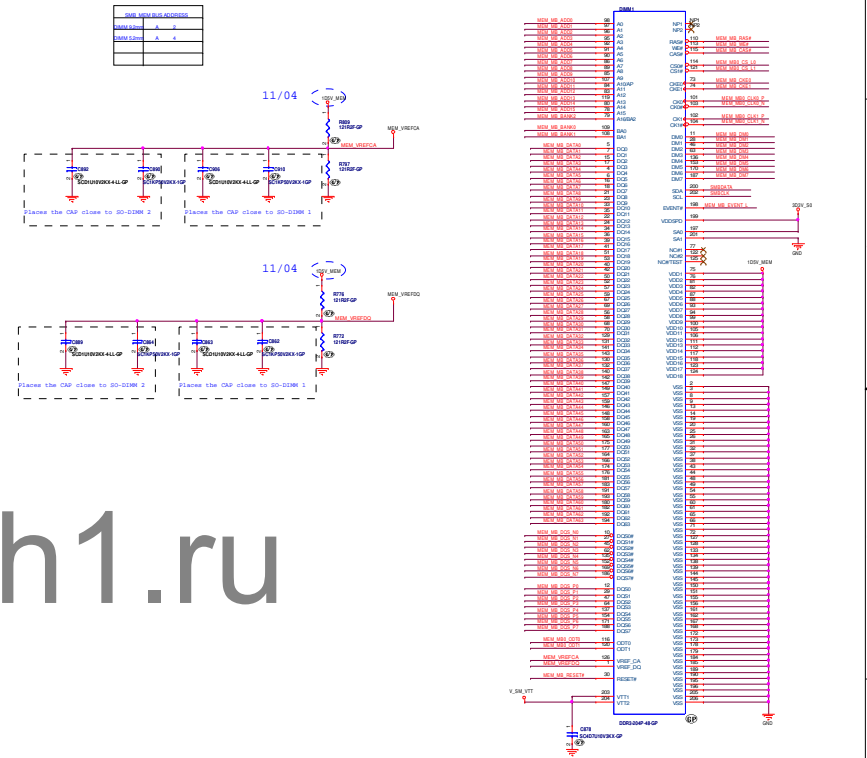
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Size A	Document Number Barbados		Rev 1B
Date:	Saturday, April 24, 2010	Sheet	20 of 62

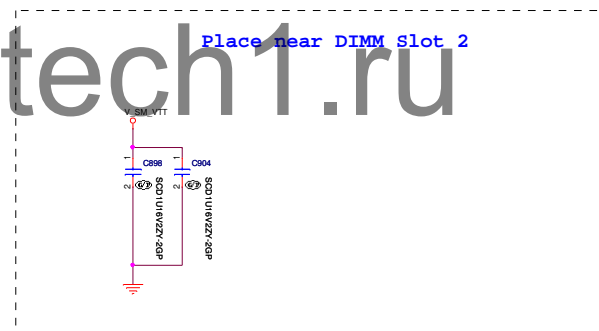
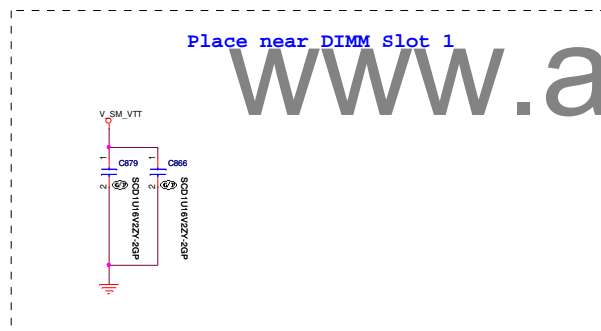
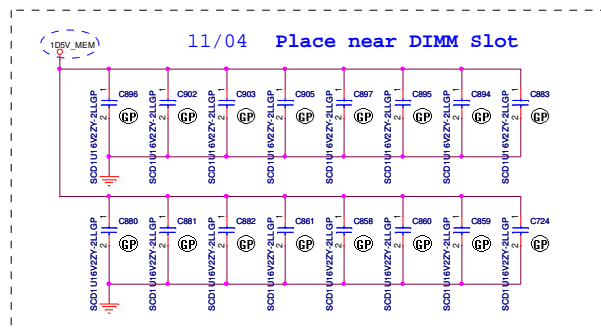


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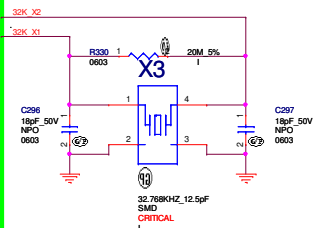


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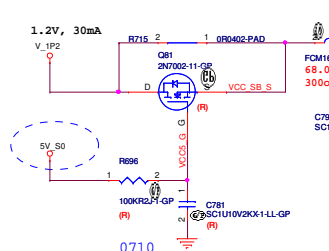




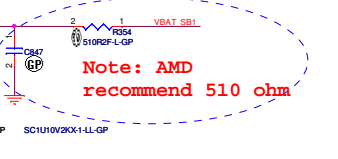
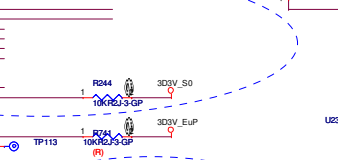
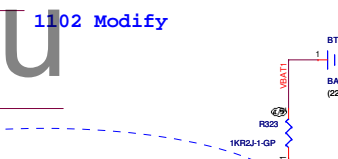
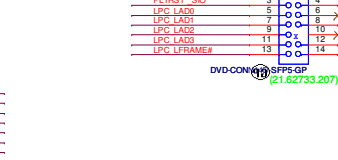
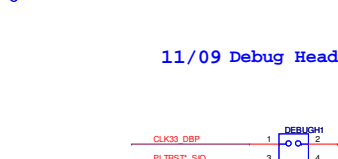
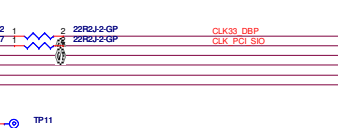
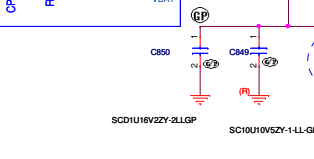
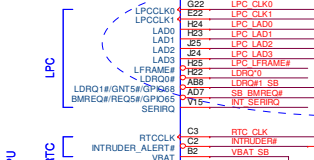
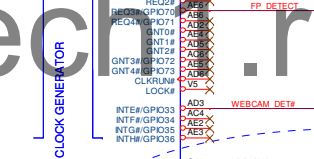
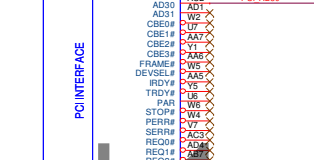
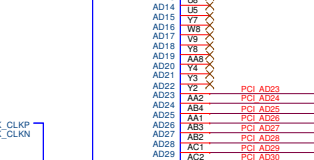
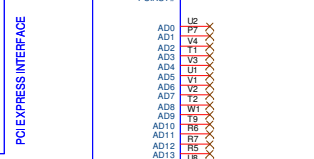
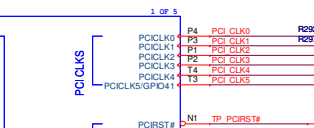
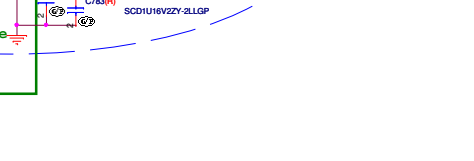
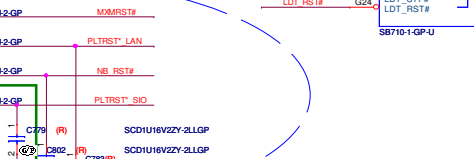
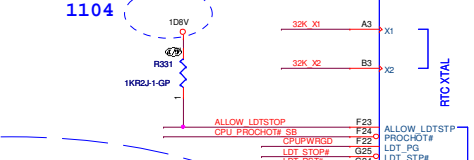
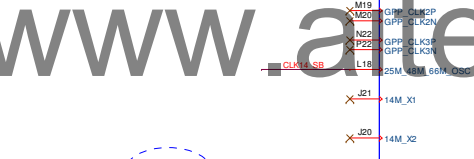
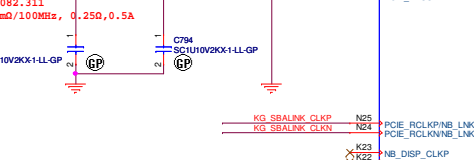
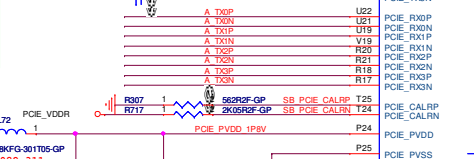
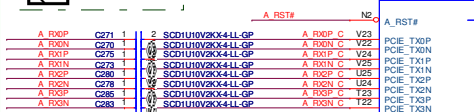
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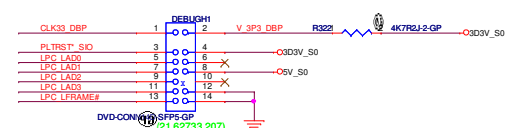
1103



Fine tune the timing



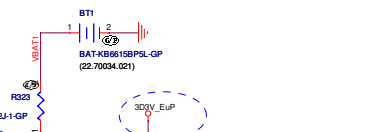
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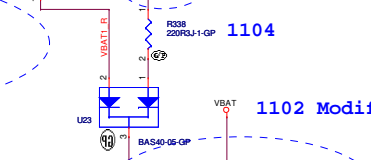
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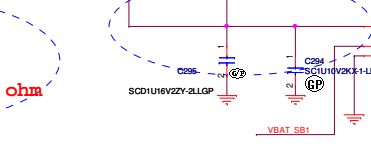
1102 Modify



1104



1102 Modify



Note: AMD recommend 510 ohm

&lt;Variant Name:



Table 4: Integrated Pull-ups and Pull-downs

Interface	Signal Name	Pull-up/down	Resistor Value (Ω)
IDE	PIDE_D0Q	Pull-down	5.6K
	PIDE_D0Q	Pull-down	5.6K +/- 20%
	PIDE_D0QY	Pull-up	4.7K +/- 20%
	PIDE_D0QY	Pull-up	4.7K +/- 20%
	PIDE_D7Q	Pull-down	10K +/- 20%
	PIDE_D7Q	Pull-down	10K +/- 20%
	PIDE_D7	Pull-down	10K +/- 20%
USB	48M_X1AUSCLK	Pull-down	50K
	USB_HSDM[7:0]	Pull-down	15K +/- 20%
	USB_HSDP[7:0]	Pull-down	15K +/- 20%
	AC_BITCLK	Pull-down	50K
AC '07	AC_SDI[2:0]	Pull-down	50K
	A23M	Pull-up	1.25K +/- 20%
Processor	CPU_PG	Pull-up	1.25K +/- 20%
	FERR#	Pull-up	1.25K +/- 20%
	ISIN#	Pull-up	1.25K +/- 20%
	INIT#	Pull-up	1.25K +/- 20%
	INTR/LINT0	Pull-up	1.25K +/- 20%
	NMI/LINT1	Pull-up	1.25K +/- 20%
	SMI#	Pull-up	1.25K +/- 20%
	STPCLK#ALLOW_LDTSTP	Pull-up	1.25K +/- 20%

PLACE SATA AC COUPLING  
CAPS CLOSE TO S600

11/10

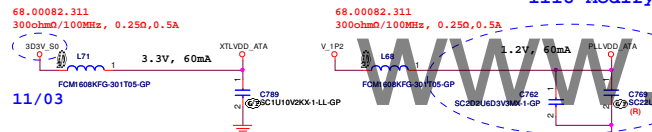
32 SATA\_TXP0\_C  
32 SATA\_TXN0\_C  
32 SATA\_RXN0\_C  
32 SATA\_RXP0\_C  
32 SATA\_TXP1\_C  
32 SATA\_TXN1\_C  
32 SATA\_RXN1\_C  
32 SATA\_RXP1\_C

**NOTE:**  
DSG-215SB600-10.pdf, page 17  
When NOT using the serial ATA interface:  
a. Leave the SATA transmit and receive pairs unconnected  
b. Leave the SATA\_ACT#, SATA\_CAL, and SATA\_X2 balls unconnected.  
c. Connect SATA\_X1 ball to GND.

**NOTE:**  
PLACE SATA\_CAL  
RES & CAP VERY  
CLOSE TO BALL  
OF U27

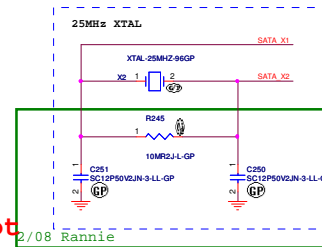
**NOTE:**  
R520 IS 1K 1% FOR 25MHz  
XTAL. 4.99K 1% FOR 100MHz  
INTERNAL CLOCK

1118 Modify



11/03

1102 Modify



2/08 Rannie

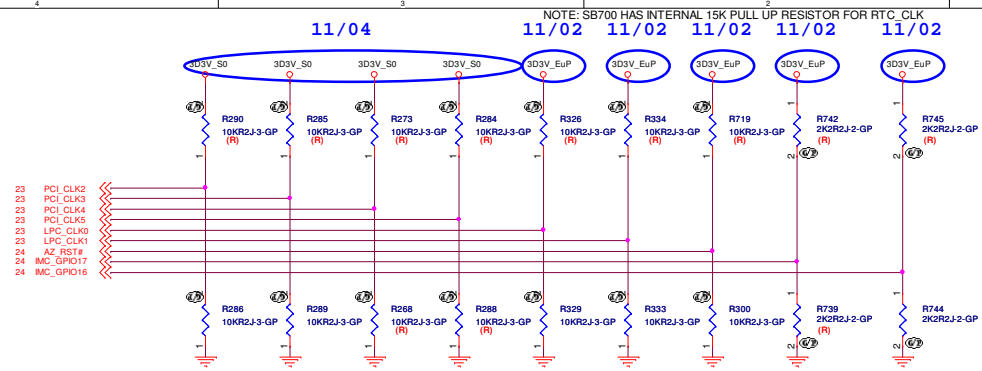
In current design, the SATA interface is not implemented. AMD recommend to tie the PLLVDD\_SATA to GND directly. (\*)

1. Main Source: 72.25X80.A01(Winbond 8Mb)
2. 2nd Source: 72.25805.001 (MXIC 8Mb)
3. 3ns source: 72.26081.001 (ATMEL 8Mb)

&lt;Variant Name&gt;

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsinchu, Taipei	
File	SB710-SATA/IDE	Document Number	Rev 18
Size	Customer	Barbados	
Date:	Revised: April 24, 2010	Sheet	25 of 82





## REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved NC, L = SPI ROM DEFAULT	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM	

2009/12/23

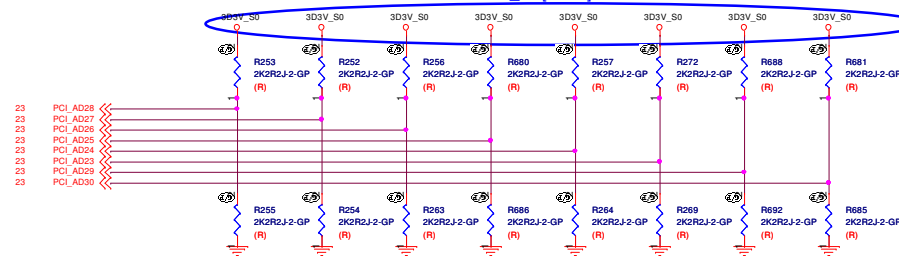


OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

## DEBUG STRAPS

11/04

SB700 HAS 15K INTERNAL PU FOR PCI\_AD[30:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD29 PCI_AD30
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED	

<Variant Name>

<b>wistron</b>		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
File SB710 STRAPS			
Size Custom	Document Number Barbados	Rev 18	
Date: Saturday, April 24, 2010		Sheet 27 of 62	





## PCH

24 ACZ\_RST#\_AUDIO >>> ACZ\_RST#\_AUDIO  
 24 ACZ\_SYNC\_AUDIO >>> ACZ\_SYNC\_AUDIO  
 24 ACZ\_SDATANI >>> ACZ\_SDATANI  
 24 ACZ\_BITCLK\_AUDIO >>> ACZ\_BITCLK\_AUDIO  
 24 ACZ\_SDATAOUT\_AUDIO >>> ACZ\_SDATAOUT\_AUDIO  
 24 ACZ\_SPKR >>> ACZ\_SPKR

## MIC JK

40 MIC\_R\_JACK >>> MIC\_R\_JACK  
 40 MIC\_L\_JACK >>> MIC\_L\_JACK

## HeadPhone

40 ALC272\_HP\_OUT\_R <<<  
 40 ALC272\_HP\_OUT\_L <<<

## SPDIF

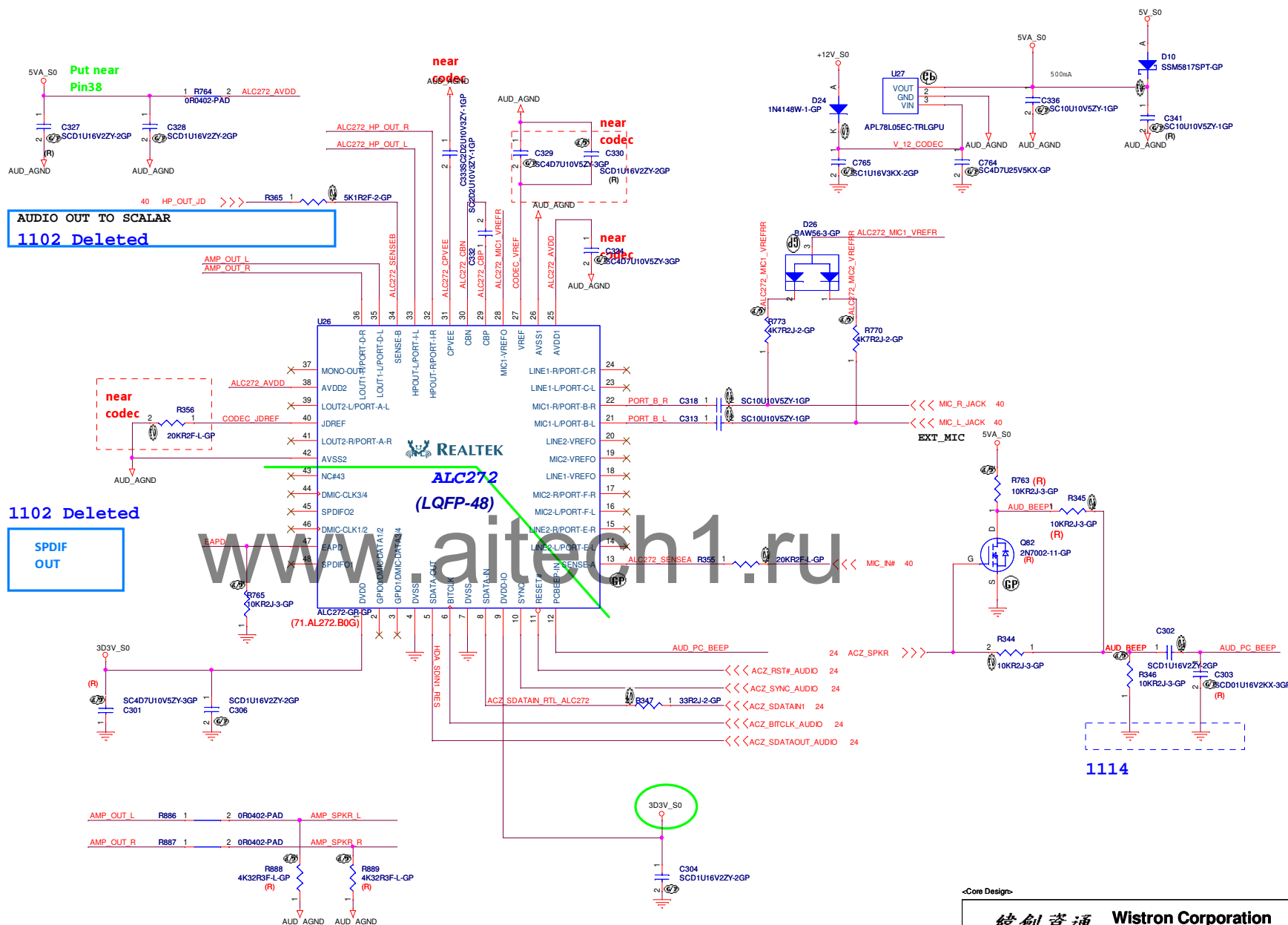
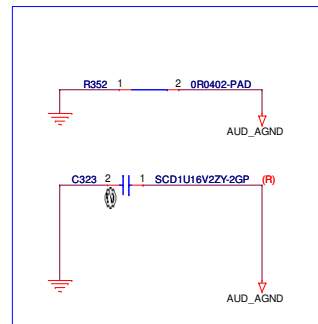


1102 Deleted  
 Jack

Detect IN# >>> MIC\_IN#  
 40 HP\_OUT\_ID >>> HP\_OUT\_ID

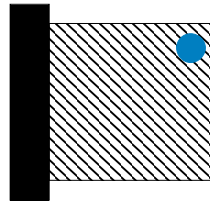
## AMP mute logic use

38 EAPD <<< EAPD  
 38 AMP\_SPKR\_L <<< AMP\_SPKR\_L  
 38 AMP\_SPKR\_R <<< AMP\_SPKR\_R

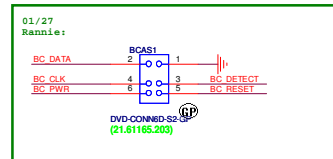
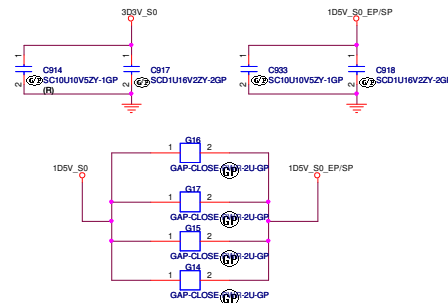
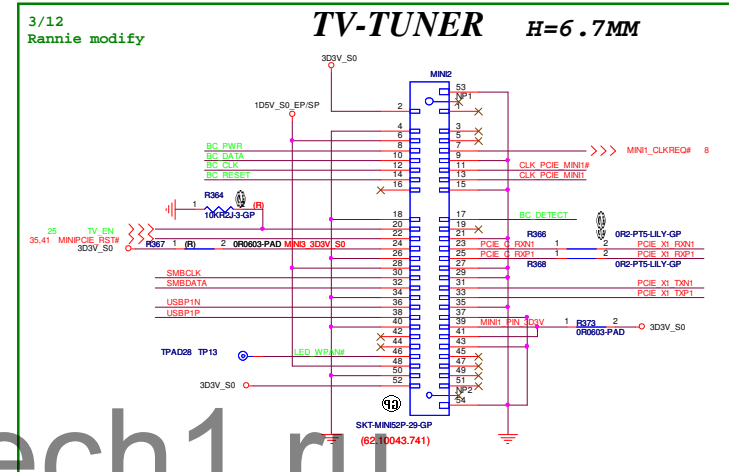
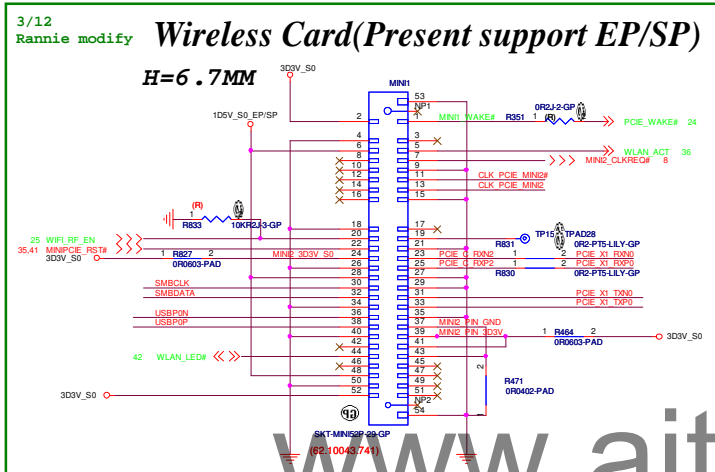
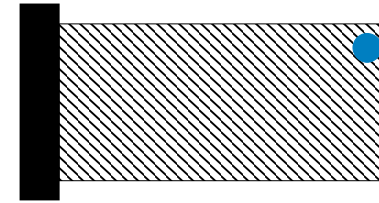


# Mini PCI-E Connector

Half Mini PCI-E CARD



Full Mini PCI-E CARD



<Variant Name>

**wistron**

Wistron Incorporated  
21F, 88, Hei Tai Wu Rd  
Hsichih, Taipei

Title		MINI PCIE Slot	
Size	Document Number	Barbados	
C		New	
Date: Saturday, April 24, 2010		Sheet	30 of 62

## RGB

17 VGA\_RED >> VGA\_RED  
17 VGA\_GREEN >> VGA\_GREEN  
17 VGA\_BLUE >> VGA\_BLUE

55 M\_RED >> M\_RED  
55 M\_GREEN >> M\_GREEN  
55 M\_BLUE >> M\_BLUE

## H/VSNC

17 VSYNC\_NB >> VSYNC\_NB  
17 HSYNC\_NB >> HSYNC\_NB

55.58 GMCH\_VSYNC >> GMCH\_VSYNC  
55.58 GMCH\_HSYNC >> GMCH\_HSYNC

## DDC\_CLK/DATA

17 VGA\_PCH\_DDCSCL << VGA\_PCH\_DDCSCL  
17 VGA\_PCH\_DDCSDA << VGA\_PCH\_DDCSDA  
55 GMCH\_DDC\_DATA << GMCH\_DDC\_DATA  
55 GMCH\_DDC\_CLK << GMCH\_DDC\_CLK

## GPIO

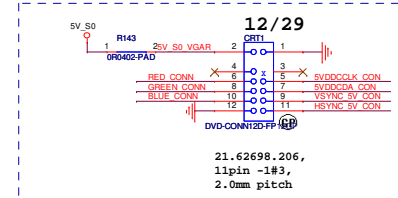
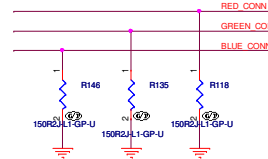
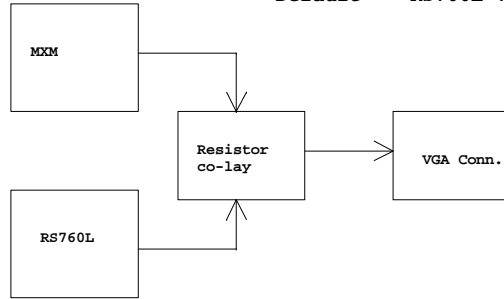
## Switch Signal to RTD2280L

28 SVDCCCLK\_CON >> SVDCCCLK\_CON  
28 SVDCCDA\_CON >> SVDCCDA\_CON  
28 VSYNC\_SV\_CON >> VSYNC\_SV\_CON  
28 HSYNC\_SV\_CON >> HSYNC\_SV\_CON  
28 RED\_CONN >> RED\_CONN  
28 GREEN\_CONN >> GREEN\_CONN  
28 BLUE\_CONN >> BLUE\_CONN

# Topology

For User Switch and Debugger

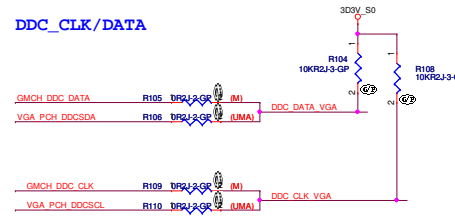
Default : RS760L VGA



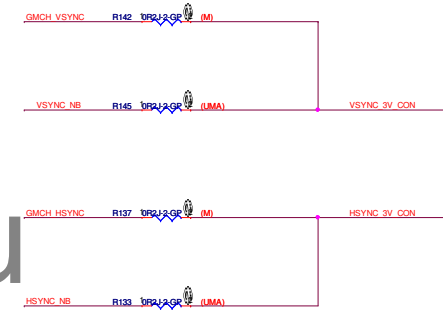
## RGB



## DDC\_CLK/DATA

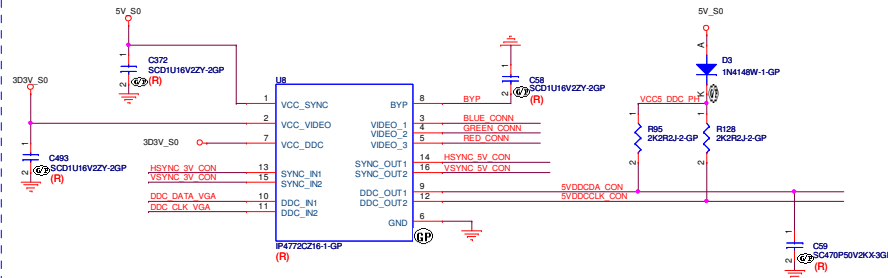


## H/VSNC



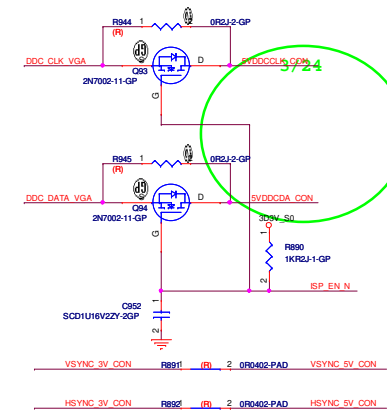
01/28

Rannie: VGA path 1



01/28

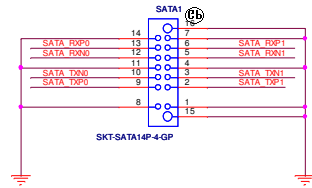
Rannie: VGA path 2



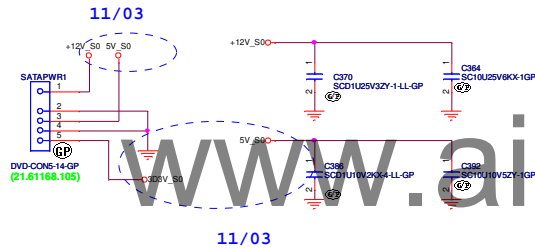
SATA\_HD

SATA\_CD\_ROM

25	SATA_RXP1_C	<<	C873	1	SC001U18V2KX3GP	SATA_RXP1
25	SATA_RXN1_C	<<	C877	1	SC001U18V2KX3GP	SATA_RXN1
25	SATA_TXP1_C	<<	C887	1	SC001U18V2KX3GP	SATA_TXP1
25	SATA_TXN1_C	<<	C884	1	SC001U18V2KX3GP	SATA_TXN1
25	SATA_RXP0_C	<<	C885	1	SC001U18V2KX3GP	SATA_RXP0
25	SATA_RXN0_C	<<	C888	1	SC001U18V2KX3GP	SATA_RXN0
25	SATA_TXP0_C	<<	C893	1	SC001U18V2KX3GP	SATA_TXP0
25	SATA_TXN0_C	<<	C891	1	SC001U18V2KX3GP	SATA_TXN0



3.5" SATA HDD power connector



Slim SATA ODD power connector

11/30

Delete ODD POWER CONN.

Because it could be combined in other conn.

www.aitech1.ru

<Variant Name>

wistron

Wistron Incorporated  
21F, 88, Hei Tai Wu Rd  
Hsichih, Taipei

Title

SATA CONN

Size

Document Number

C

Barbados

Rev

18

Date

Saturday, April 24, 2010

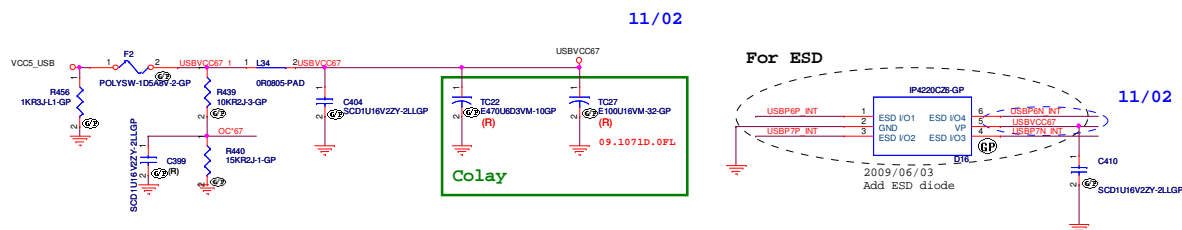
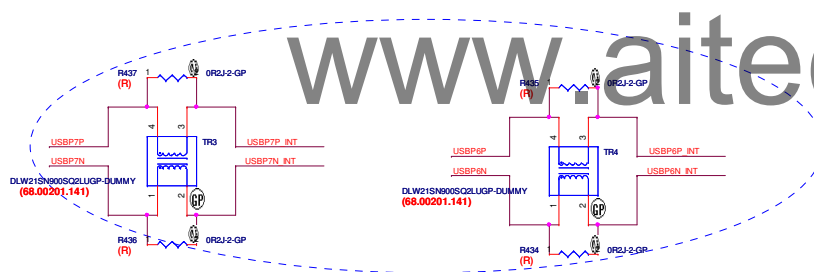
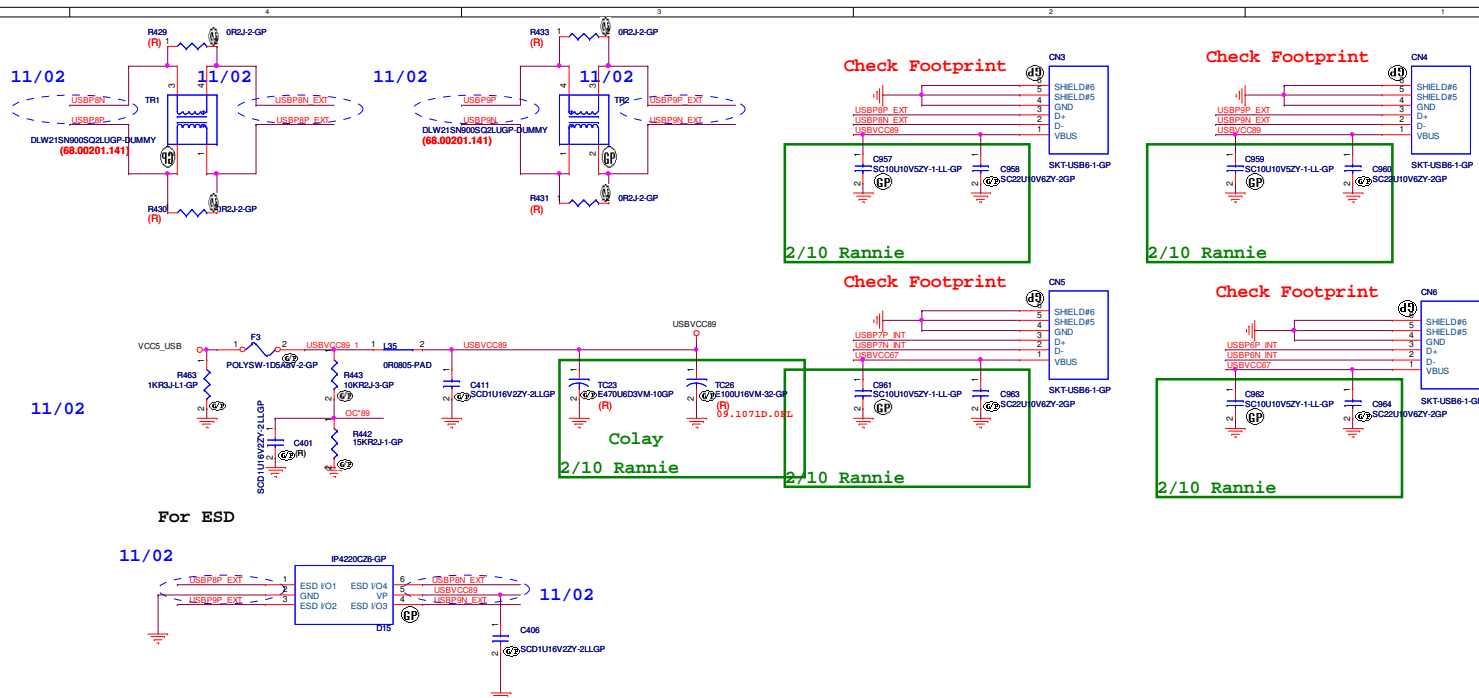
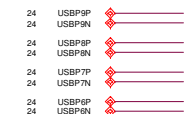
Sheet

32

of

62

USB PORT X4



24 USBP11P  
24 USBP11N  
24 USBP10P  
24 USBP10N

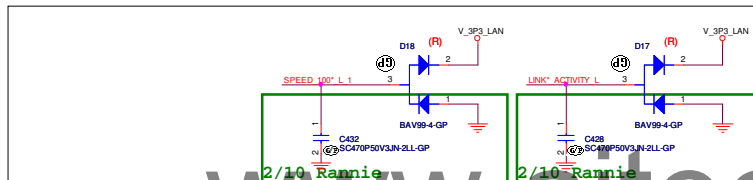
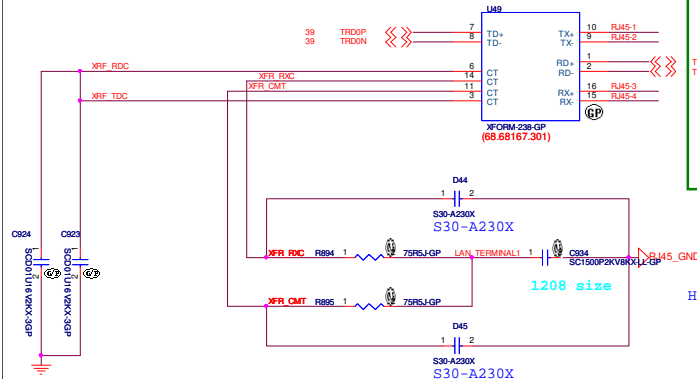
24 OC1011  
25 LAN\_100LED\_CTRL  
25 LAN\_LINKLED\_CTRL

39 SPEED\_100\_L  
39 SPEED\_100\_L  
39 LINK\_ACTIVITY\_L

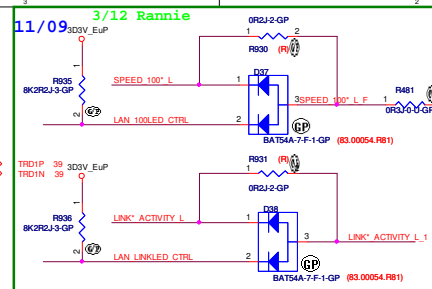
39 TRDOP  
39 TRDON  
39 TRDIP  
39 TRDIN

01/29  
Lenovo suggestion

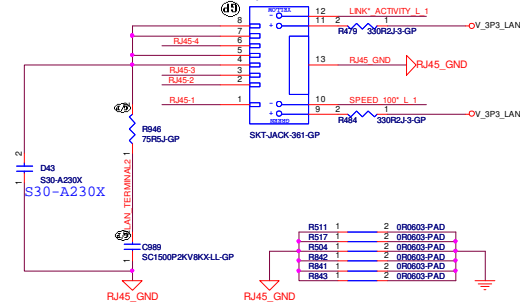
10/100M Lan Transformer



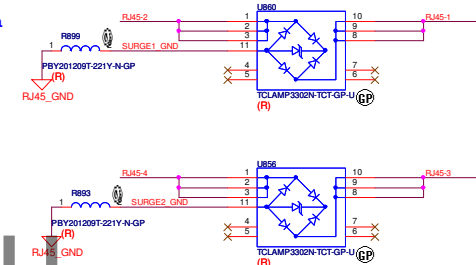
H16 connected to GND for LAN ESD protector



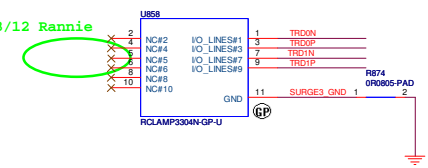
Check Footprint 2010/01/05



2010/01/05  
LAN Surge Solution

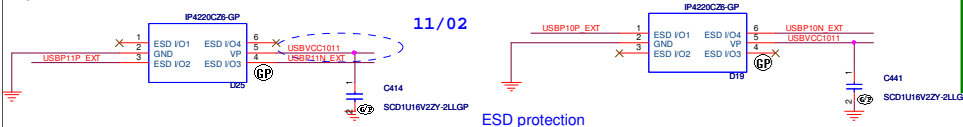


3/12 Rannie



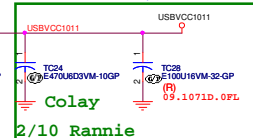
Side 2 USB PORT  
(2/3)

For ESD

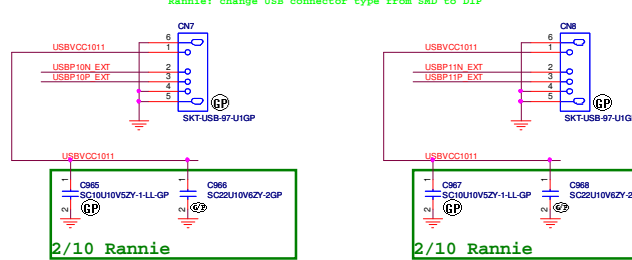


Colay  
2/10 Rannie

11/02



01/27  
Rannie: change USB connector type from SMD to DIP



2/10 Rannie

2/10 Rannie

<Variant Name>

wlstron

Wistron Incorporated  
21F, 88, Hein Tai Wu Rd  
Hsieh, Taipei

FRONT USBX2 + RJ45

Barbados

Date: Sunday, April 25, 2010

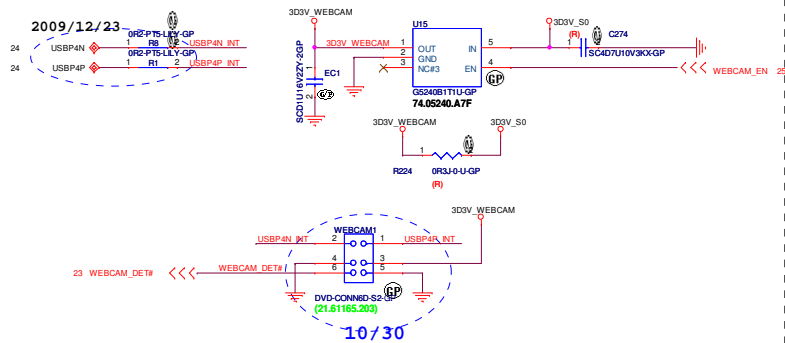
Sheet 34 of 62



## CAMERA

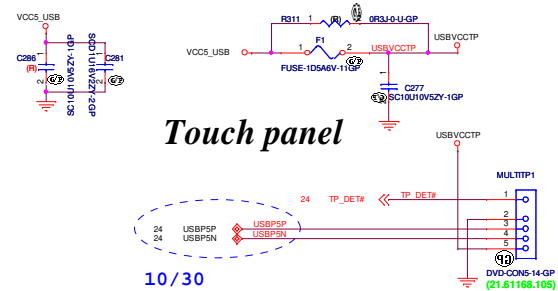
10 / 30

2009/12/23



WEBCAM	WEBCAM Function
L	Cable inserted
H	Cable not inserted

nextwindow 1950 series

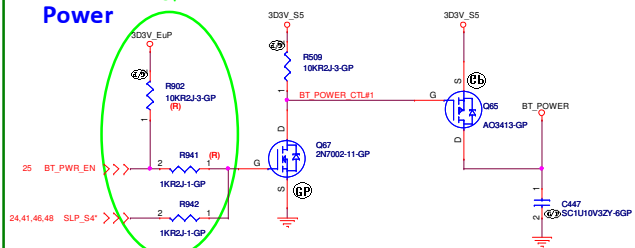


TP_DET#	Nextwindow Function
L	Cable inserted
H	Cable not inserted

0201 Rannie modify

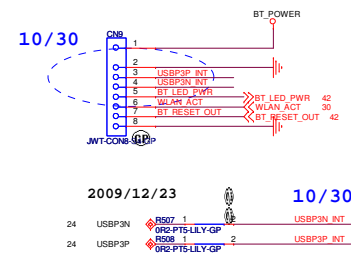
**Blue  
Tooth  
Power**

3/24



BT_PWR_EN GPIO51(S5 power)	Blue Tooth Power
L	Disable
H	Enable

Blue  
Tooth

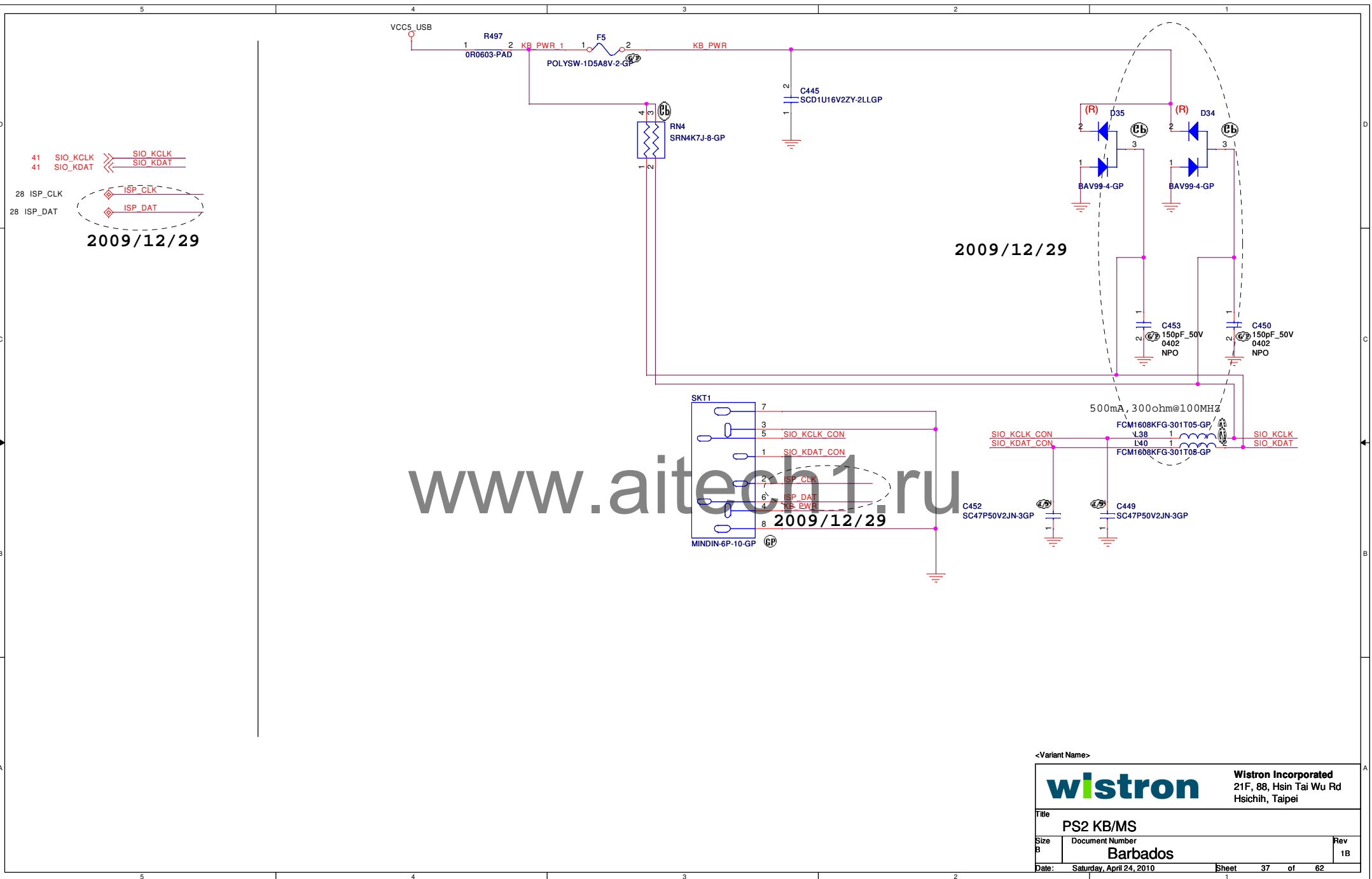


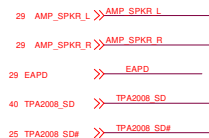
2009/12/23 10/30

24 USBP3N ◆ R507 1 ◆ OR2-PTS-LILY-GP ◆ USBP3N INT

24 USBP3P ◆ R508 1 ◆ OR2-PTS-LILY-GP ◆ USBP3P INT







16 PCIE\_GLAN\_RXP << PCIE\_GLAN\_RXP 1 C395 PCIE\_LAN\_TXP\_ICH  
SCDU10V2KX4-LL-GP

16 PCIE\_GLAN\_RXN << PCIE\_GLAN\_RXN 1 C384 PCIE\_LAN\_TXN\_ICH  
SCDU10V2KX4-LL-GP

16 PCIE\_GLAN\_TXP >> PCIE TxP LAN

16 PCIE\_GLAN\_TXN >> PCIE TxN LAN

8 KG\_GFX\_CLKP >>> \_\_\_\_\_

8 KG\_GFX\_CLKN >>> \_\_\_\_\_

23 PLTRST\* LAN >>>

24 WOL >>

34 TRD0P << TRD0P

34 TRD0N << TRD0N

34 TRD1P << TRD1P

34 TRD1N << TRD1N


[illegible]

Close to Pin 10,13,30,36

1. The trace length between R105 and 8103EL pin1 must be within 200mil.
2. C57 to R584 must be within 200mil.
3. The trace width from VDD33 to pin45 should>40mils.
4. Power plane for pin48 and around ground trace.

1. Pin48 should be near R449, and then 0.1uF(C56).
2. Pin 45 should be near 0.1u F(C57).

Need to check F/W.



Default Value of LEDS1,0 = 11

2/08 realtek suggestion

# MIC IN

To  
Codec

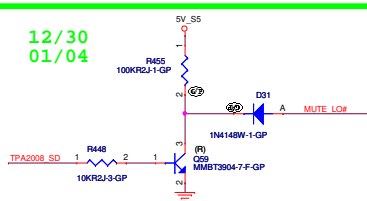
# HP

Out  
Scaler

# JACK DETECT

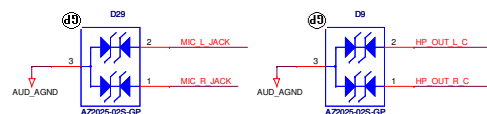
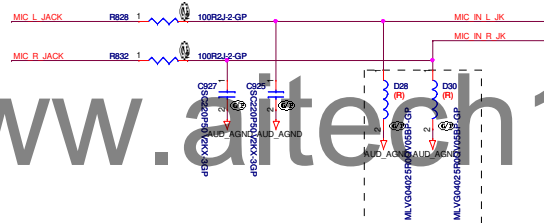
29 MIC\_IN >> MIC\_IN  
29 ALC272\_HP\_OUT\_L >> ALC272\_HP\_OUT\_L  
29 ALC272\_HP\_OUT\_R >> ALC272\_HP\_OUT\_R  
29 HP\_OUT\_ID >> HP\_OUT\_ID  
38 TPA2008\_SD >> TPA2008\_SD

12/30  
01/04



TPA3113_SD(GPIO52)	HEADER PHONE
L	Enable
H	Disable

# MIC IN

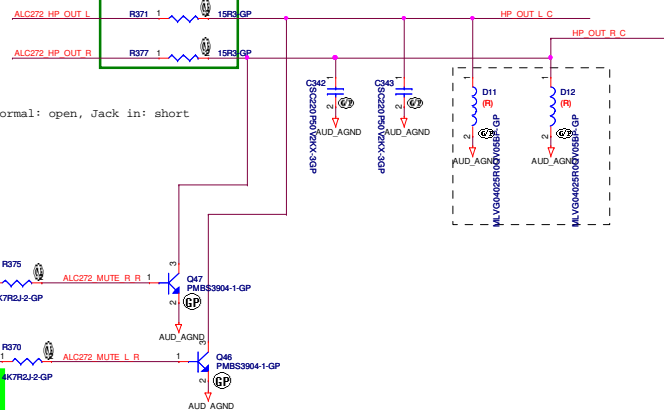


If use:  
83.02025.0A1

If use:  
83.02025.0A1

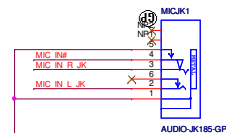
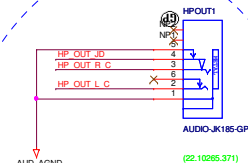
# HP OUT

2/05 rannie modify



Normal: open, Jack in: short

Check  
Footprint



<Variant Name>

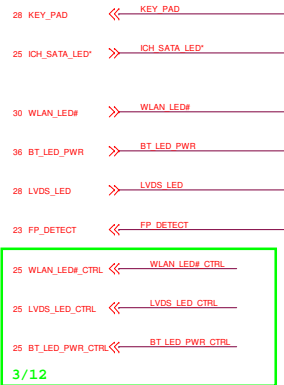
**wistron**

Wistron Incorporated  
21F, 88, Hei Tai Wu Rd  
Hsichih, Taipei

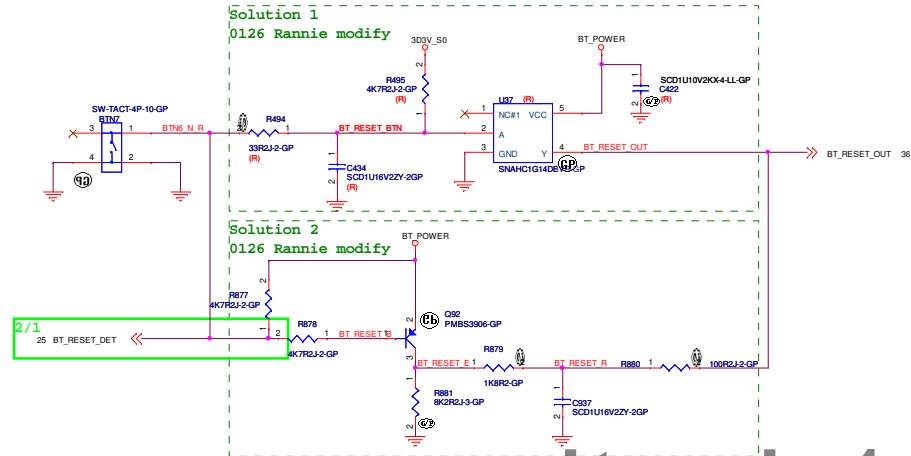
POWER DELIVERY CHART

Size C Document Number Barbados  
Date: Saturday, April 28, 2010 Sheet 40 of 62



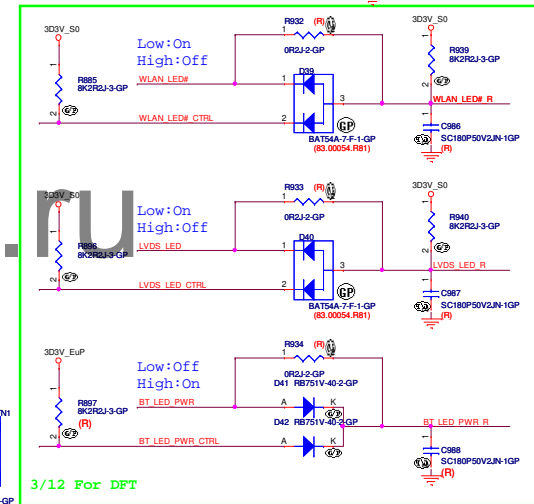
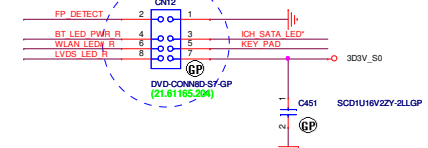


FP\_DETECT H : FP not inserted (Internal Pull-High)  
FP\_DETECT L : FP inserted



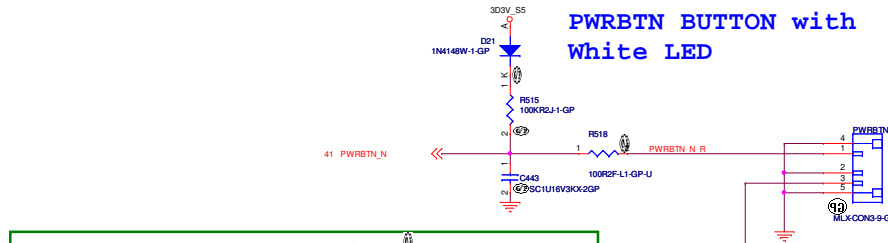
FP_DETECT	FP Cable
L	Cable inserted
H	Cable not inserted

SB-Lily requested.



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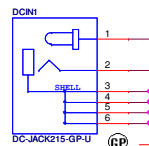
PWRBTN BUTTON with White LED



File	Block Diagram
Size	Document Number
C	Key_Pad/LED/PWRBTN
Date:	Saturday, April 24, 2010
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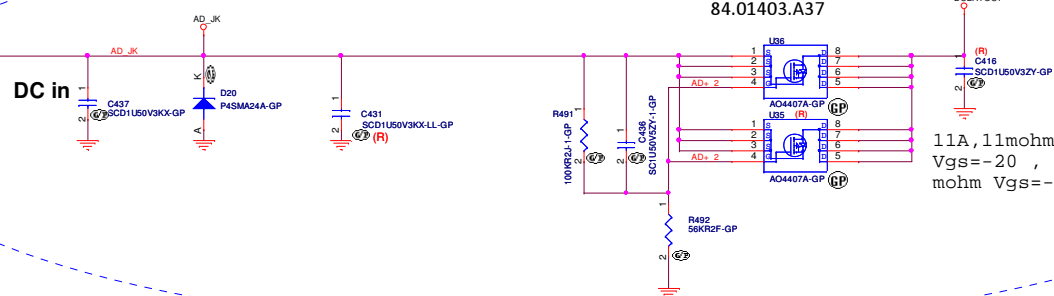
## 2/03 Rannie modify

Adaptor IN



## Adaptor in to generate DCBATOUT

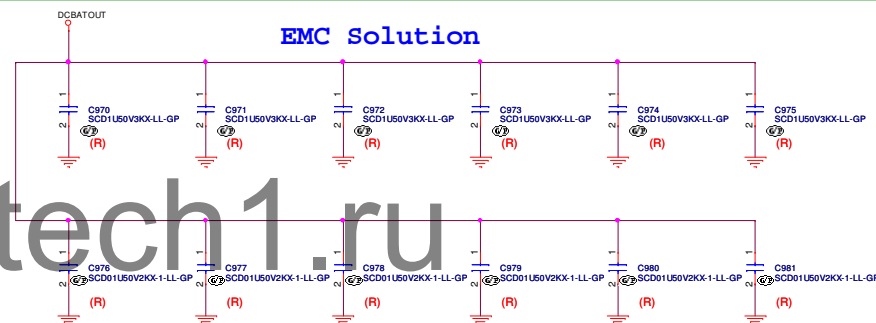
Add alternate  
84.01403.A37



11A, 11mohm < 14mohm  
Vgs = -20, 14mohm < 18  
mohm Vgs = -10

1107 Modify  
Wistron pattern

## EMC Solution



2/10 Rannie

<Variant Name>

**wistron**

Wistron Incorporated  
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Hsichih, Taipei

File  
ATX/PCIRST/SPI

Size  
Custom  
Document Number  
Barbados

Date: Saturday, April 24, 2010

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Rev  
1B

3 / 22





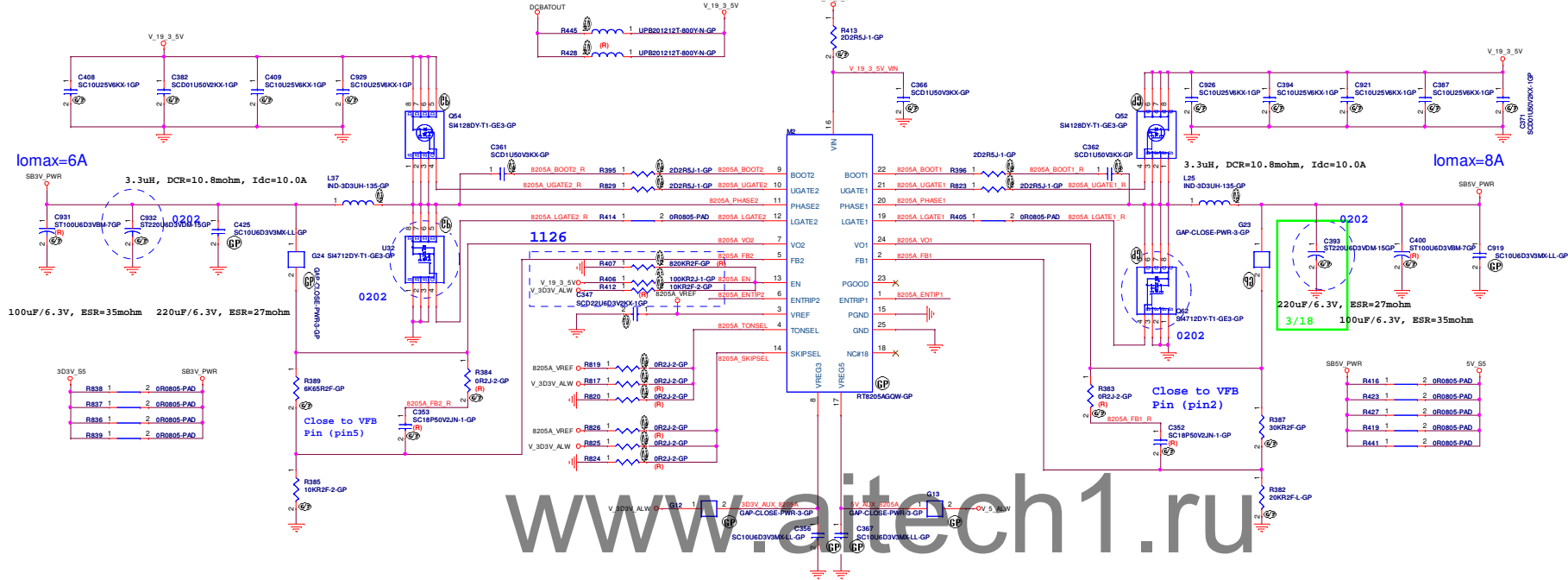
# +3VSB/+5VSB

84.04128.037 SI4128DYP  
Vgs @ 4.5V,  
Id = 6.0A,  
Rds(on) = 24.0~30.0mohm,  
Qg = 3.8~6.0nC

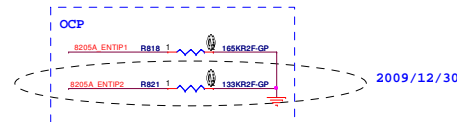
84.04712.A37 SI4712DY  
Vgs @ 4.5V,  
Id = 8.2A,  
Rds(on) = 13.0~16.5mohm,  
Qg = 8.3~12.5nC

84.04128.037 SI4128DYP  
Vgs @ 4.5V,  
Id = 6.0A,  
Rds(on) = 24.0~30.0mohm,  
Qg = 3.8~6.0nC

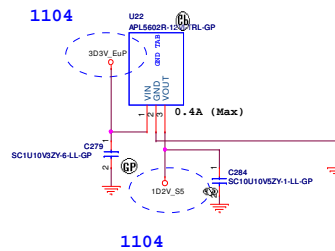
84.04712.A37 SI4712DY  
Vgs @ 4.5V,  
Id = 8.2A,  
Rds(on) = 13.0~16.5mohm,  
Qg = 8.3~12.5nC



	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	SKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	330k/CH1 375k/CH2	400k/CH1 500k/CH2	400k/CH1 500k/CH2



## USB\_PHY\_1.2VSB Place near SB

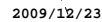


<Core Design>

It might be cost down in SB.



11/16 Modify



11/02 Modify



IDmax =0.75A  
For Mini-PCIE

11/02 Modify

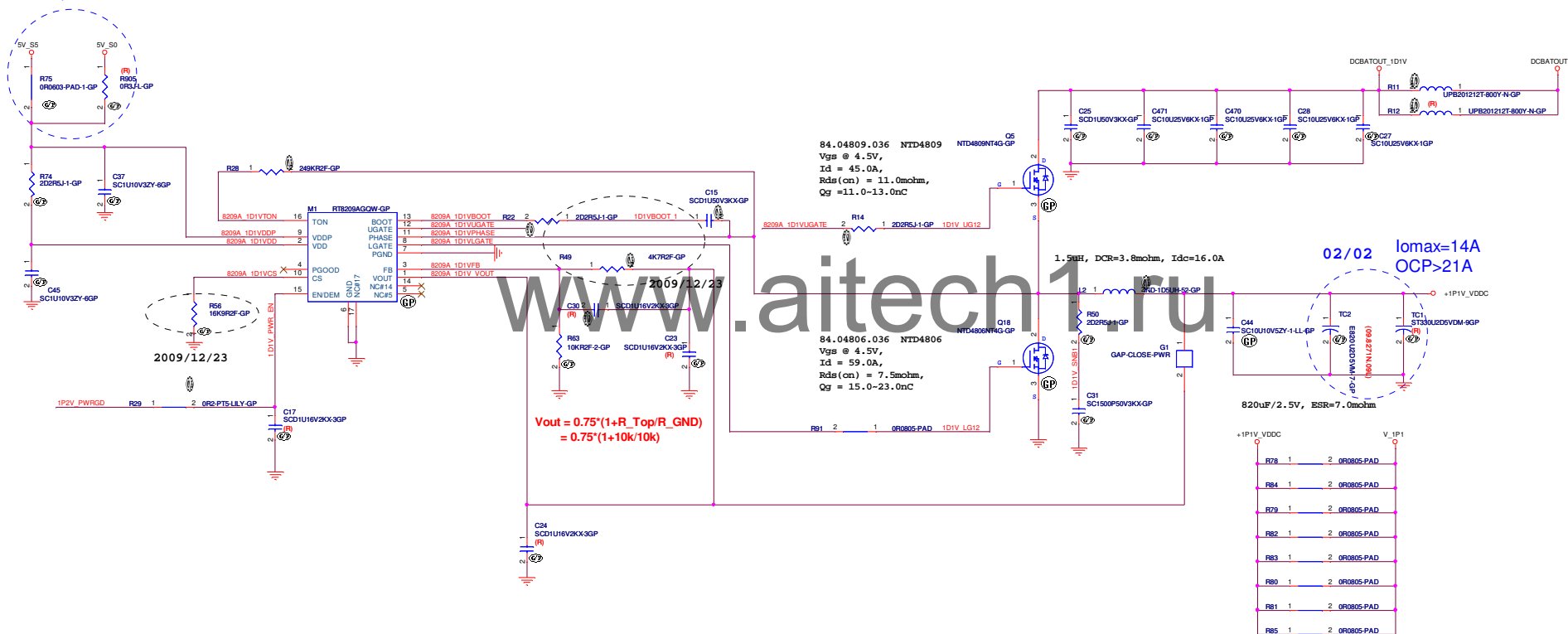


IDmax = 6A  
For USB

8.49 1P2V\_PWRGD >> 1P2V\_PWRGD

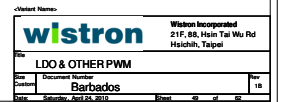
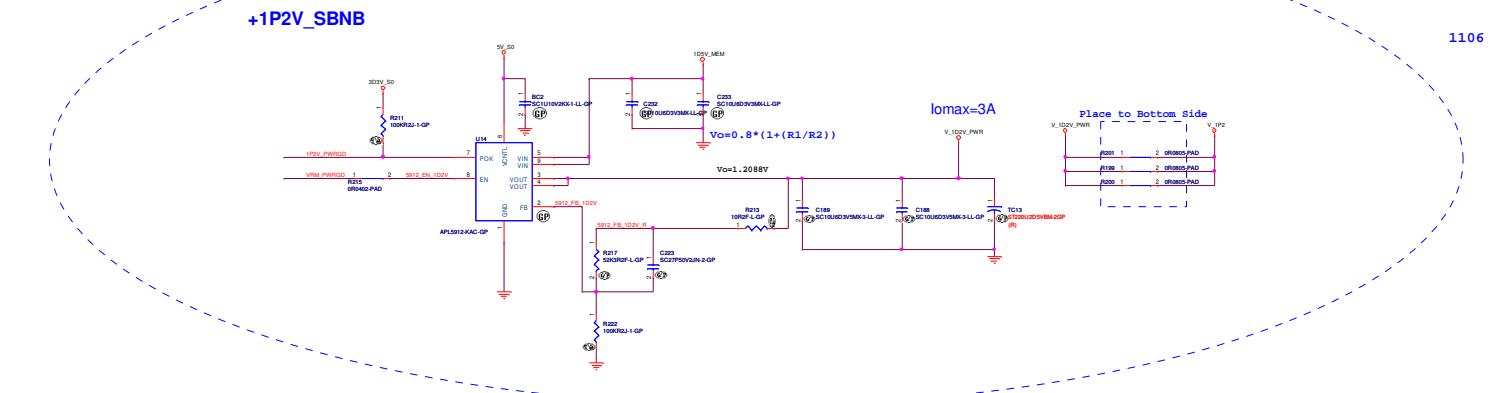
+1P1V\_VDDC(NB)

02/02



11/06

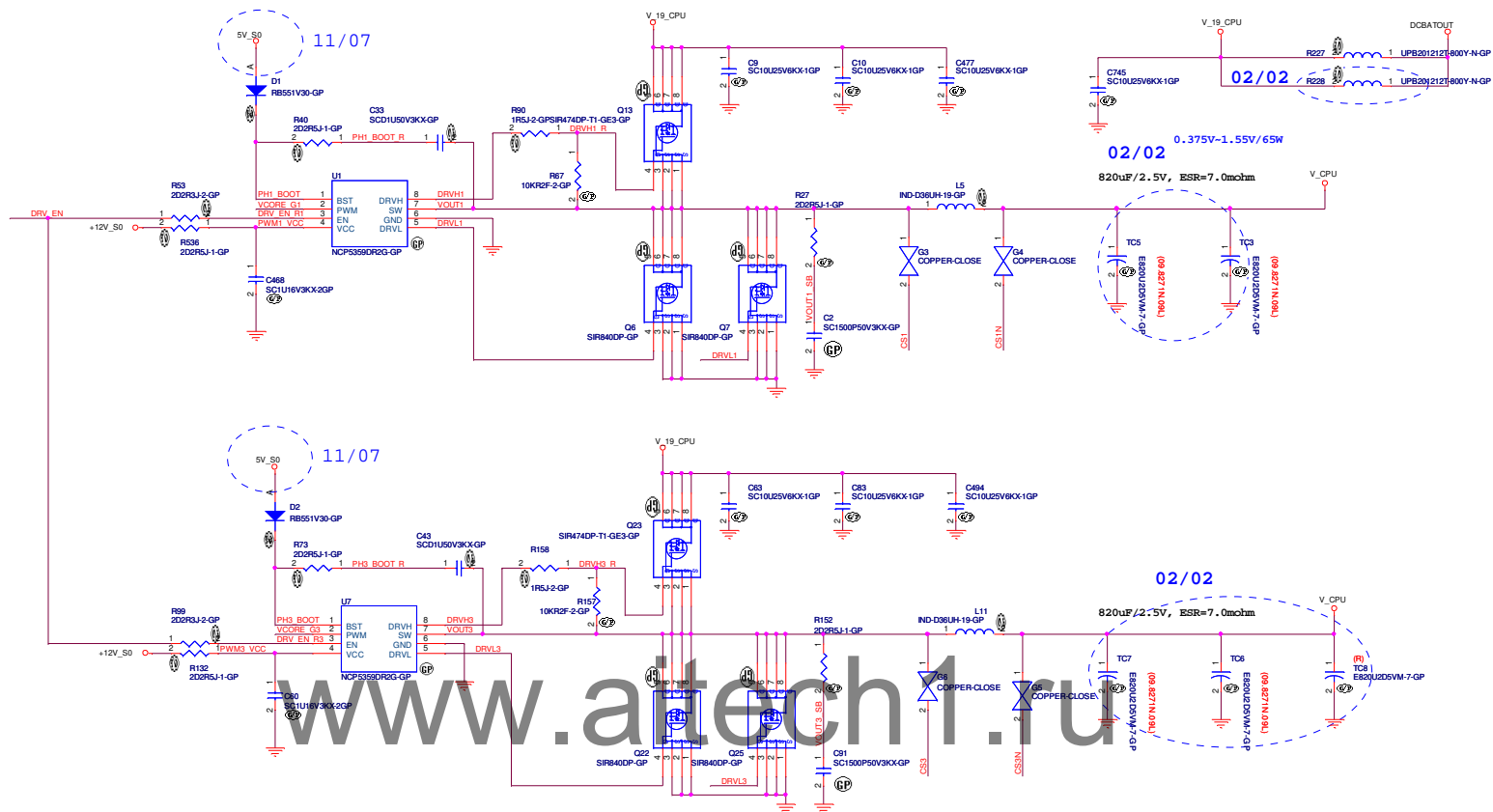






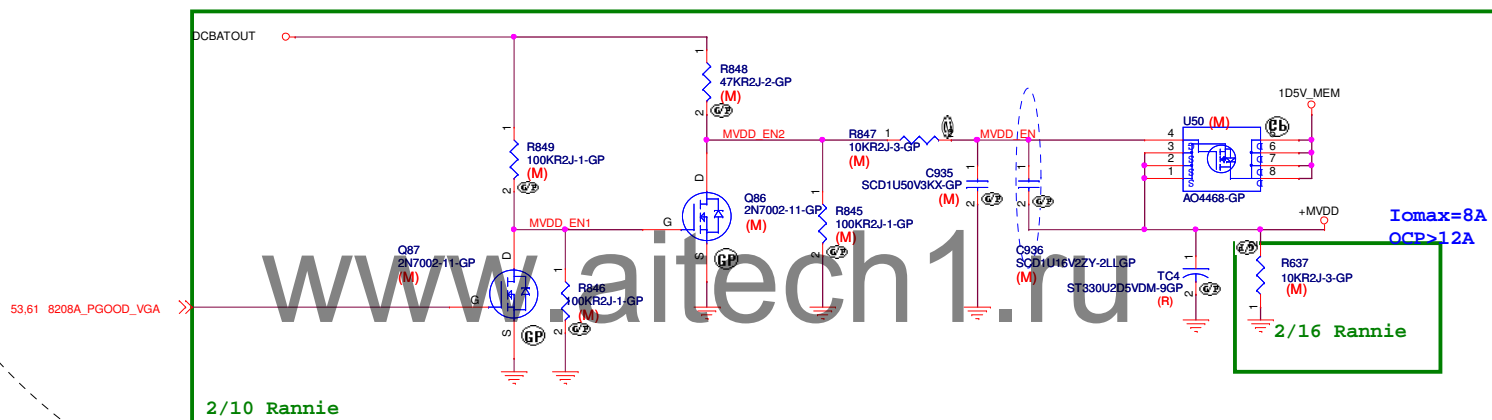
50 DRV\_EN >> DRV\_EN  
50 VCORE\_G1 >> VCORE\_G1  
50 CS1 >> CS1N  
50 CS3N >> CS3N

50 VCORE\_G3 >> VCORE\_G3  
50 CS3 >> CS3  
50 CS3N >> CS3N



<Variant Name>

2009/12/23



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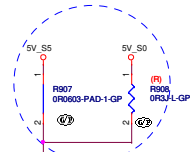
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title RT8209E\_1D5V\_VRAM

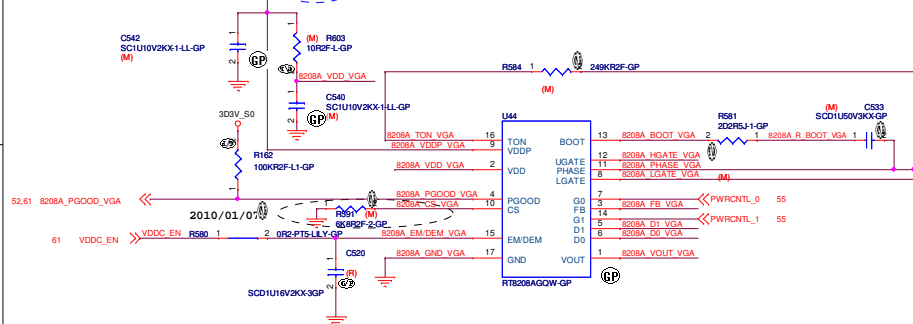
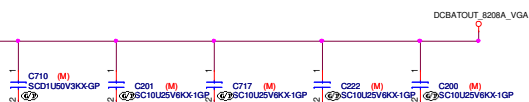
Size A3	Document Number JV71-TR8	Rev 1B
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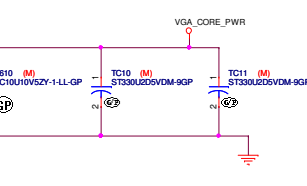
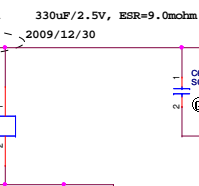
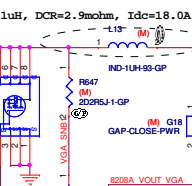
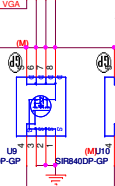
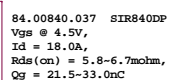
## RT8208A for VGA



84.00474.037 SIR474DP  
Vgs @ 4.5V,  
Id = 12.0A,  
Rds(on) = 10.0~12.0mohm,  
Qg = 8.0~12.0nC

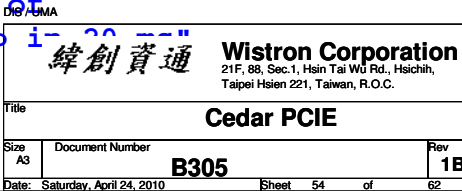


1uH, DCR=2.9mohm, Idc=18.0A      330uF/2.5V, ESR=9.0mohm



GPIO20/G1	GPIO15/G0	
PWRCNTL_1	PWRCNTL_0	Voltage
1	1	1.12V
1	0	1.07V
0	1	0.95V
0	0	0.9V

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## Check!!

DVPDATA [3:2:1:0] for VRAM type  
selection H/W strap  
Should provide VRAM Table for VBios  
request

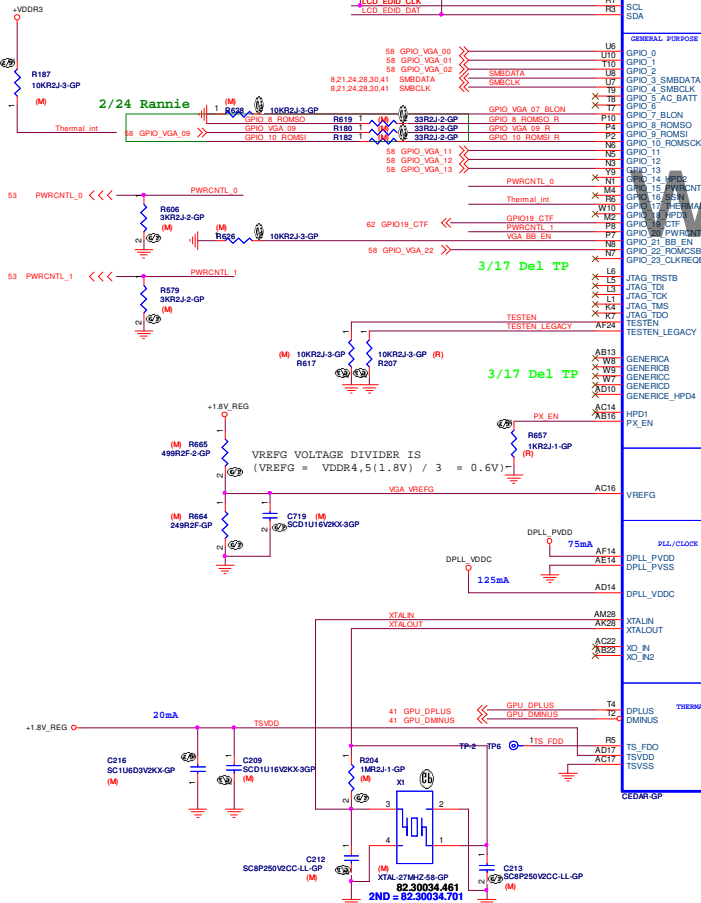
DVPDATA [3:0]  
0000 512MB DDR3 Hynix-H5TQ1G63BFR-12C (800MHz)  
0001 512 DDR3 Samsung-K4W1G1646E-HC12 (800MHz)

DVPDATA [11:0]  
DVD pixel bus.  
Initialization Behavior: These signals are inputs  
during reset (no reference clock is required). After  
reset, the default states are output low (0 V).

Internal pull-down

Must be tied high if not used.

It's strap for GDDR3-136ball  
Need to Clarify



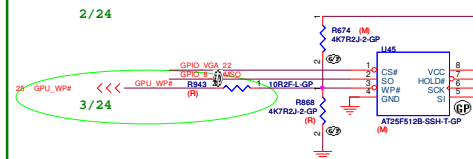
## Integrated TMDs2 Interface

Note:

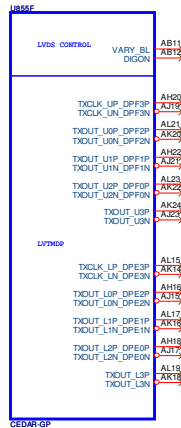
- If this interface is not used, all signal outputs can be unconnected. Power, ground, and DPxx\_CALR MUST remain connected.

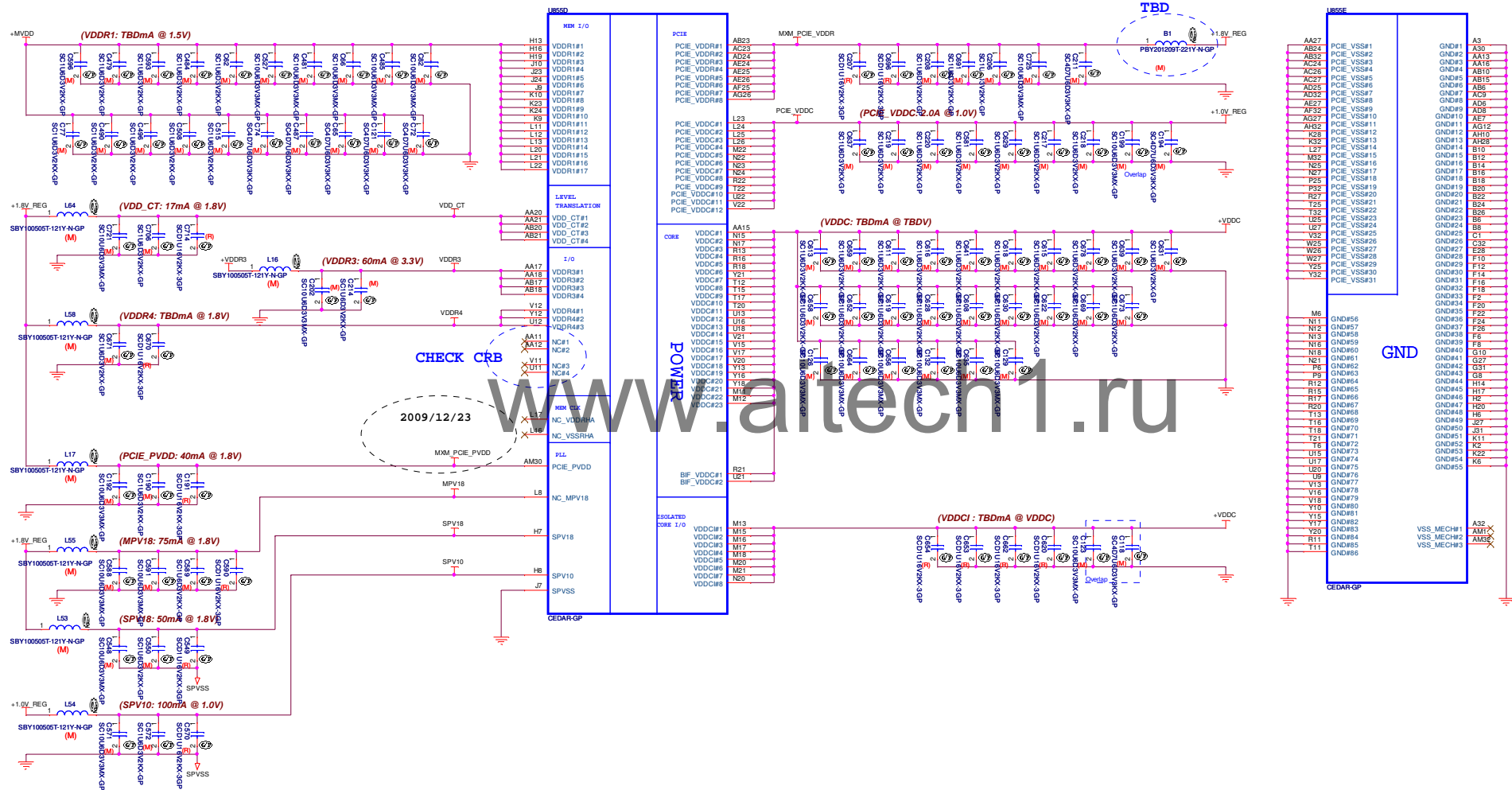
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## SERIAL EEPROM 512K/1M



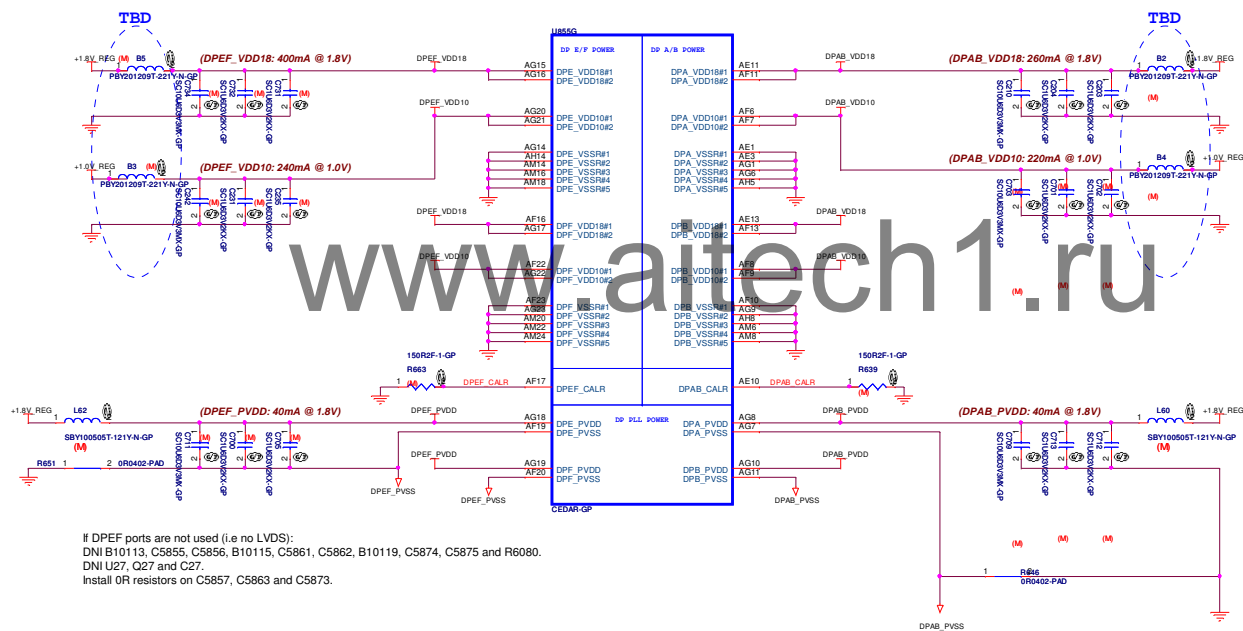
A 256MB MEMORY APERTURE SIZE  
CAN BE DEFINED USING A SEPARATE  
ROM OR STRAPPING





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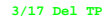
Cedar IO		
File	Document Number	Rev
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DSB/UMA

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsinchu 301, Taiwan, R.O.C.	
<b>DP POWER_GND</b>	
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DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



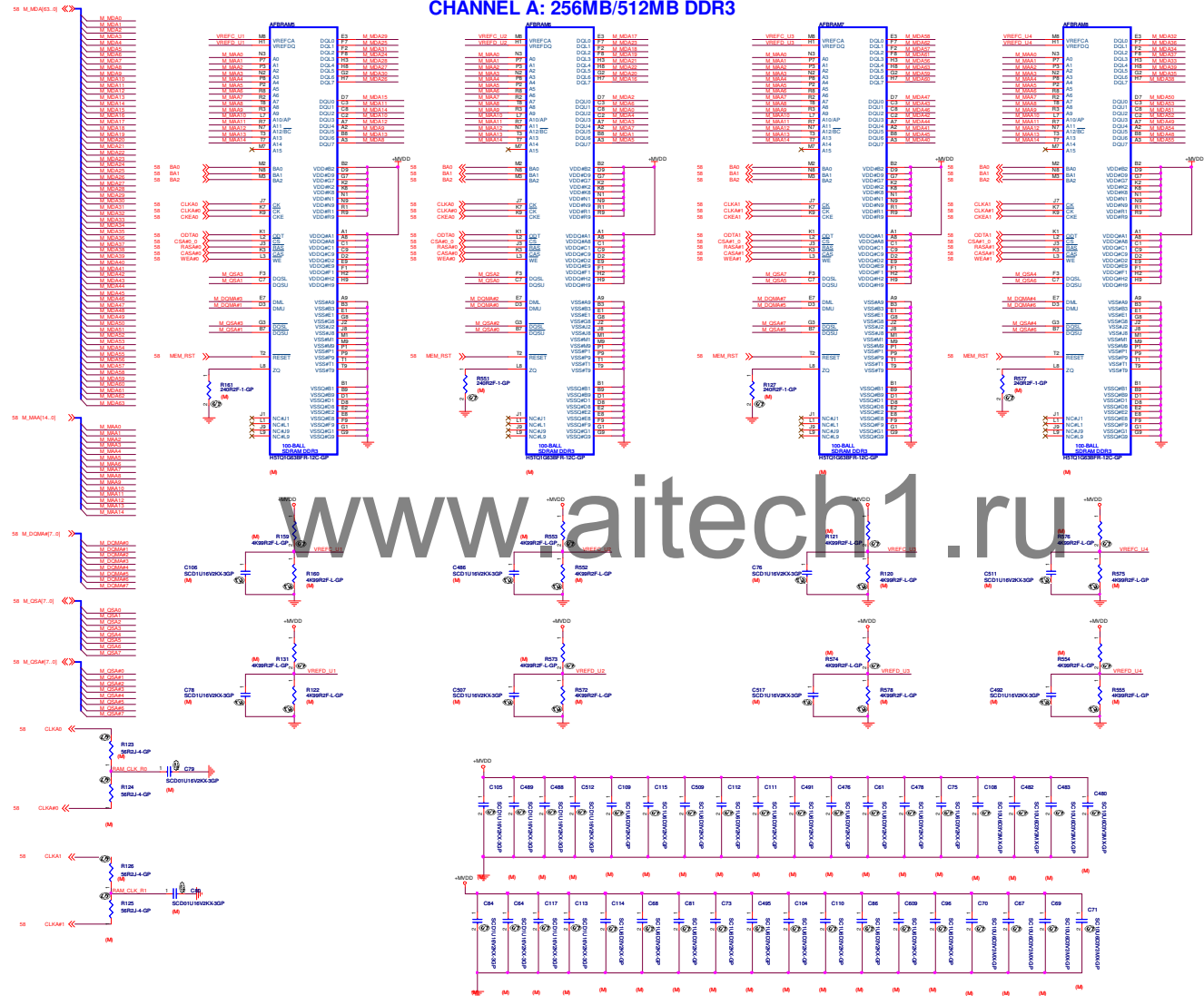
## PIN STRAPS



STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0.50% Tx output swing (Internal Pull-down) 1: Full Tx output swing	GPIO0 and GPIO1 pulls up, need to be stuffed with G5536 if system board is controlling the PCIe swing. 1
TX_DEEMPH_EN	GPIO1	TX Transmitter De-emphasis Enable 0: Tx de-emphasis disabled (Internal Pull-down) 1: Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIe Gen2 Enable 0: Advertises the PCIe device as 2.50GT/s capable at power-on (Internal Pull-down) 1: Advertises the PCIe device as 5.00GT/s capable at power-on	1
BIF_VGA_DIS	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	GPIO9 pull up needs to be stuffed with G5537 if system board is controlling the VGA capacity 0
ROMDCFG2[2]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO2 = 0, defines memory aperture size If GPIO2 = 1, defines ROM type 101: 32Mbit ROM type (ST) 100: 128Mbit ROM type (ST) 101: 32Mbit ROM type (ST) 100: 48Mbit ROM type (ST) 101: 32Mbit ROM type (ST) 100: 32Mbit ROM type (Cypress) 101: 1Mbit ROM type (Cypress)	(Internal Pull-down) XXX
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	(Internal Pull-down) 0
AUD[1] AUD[0]	H5VNC V5VNC	00: No audio function 01: Audio for DP only 10: Audio for DP and HDMI display is detected 11: Audio for both DP and HDMI HDMI must only be enabled on systems that are legally certified. It is the responsibility of the system designer to ensure that the system is certified to support this feature.	XX
VP_DEVICE_STRAP_ENA	V5VNC	VP Device Strap Enable 0: Slave VP host port devices present 1: Slave VP host port devices reporting presence	(Internal Pull-down) 0
Reserved	H2VNC	Reserved  Internal use only. This PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected, however, if it is connected to additional logic on the board, the logic must not allow this signal to be driven or pulled to any value except GND at reset.	0

72.51G63.C0U gDDRIII 64M\*16 800MHz VRAM 54nm (Orion die) FBGA96P HYNIX H5TQ1G63BFR-12C  
72.41164.H0U gDDR3 64M\*16 800MHz VRAM E die FBGA 96P SAMSUNG K4W1G1646E-HC12

# CHANNEL A: 256MB/512MB DDR3



Reserved  
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Title **VRAM Rank 2 (Reserve)**

Size A3	Document Number <b>B305</b>	Rev <b>1B</b>
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## = (not to scale)



+5V RUN

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PWR\_EN

+VDDR3

VDRG

PWR EN

H : Fine  
L : Over-temperature

H : System Power rail up sucessfully  
L : System Power rail up fail

**VDDR3, A2VDD** +VDDR3 should ramp before or simultaneously with +VDDC. +VDDC should ramp before +1.8V<sub>REG</sub> and +1.0V<sub>REG</sub>.

VDDC, VDDC

VDDR1, MVDDQ/C

VDDR4, VDD\_CT, TSVDD, PCIE\_VDDR, PCIE\_PVDD, DPLL\_PVDD, DPx\_PVDD,  
DPx\_VDD18 MPV18 SPV18, AVDD, VDD1DI, A2VDDQ, VDD2DI,

PCIE\_VDDC, DPLL\_VDDC, DPx\_VDD10, SPV10

**+1.0V\_REG AND +1.8V\_REG RAMP UP SEQUENCE CAN BE INTERCHANGED**

+1P8V For GPU

 $I_{\text{max}} = 1.3 \text{ A}$ 

**+1.0V\_REG**  
Iomax=1.7A

02/02

2009/12/2

2009/12/23

2009/12/23

Vo=0.8\*(1+(R1/R2))  
High Enable

02/02

$$R1/R2 = 0.25$$

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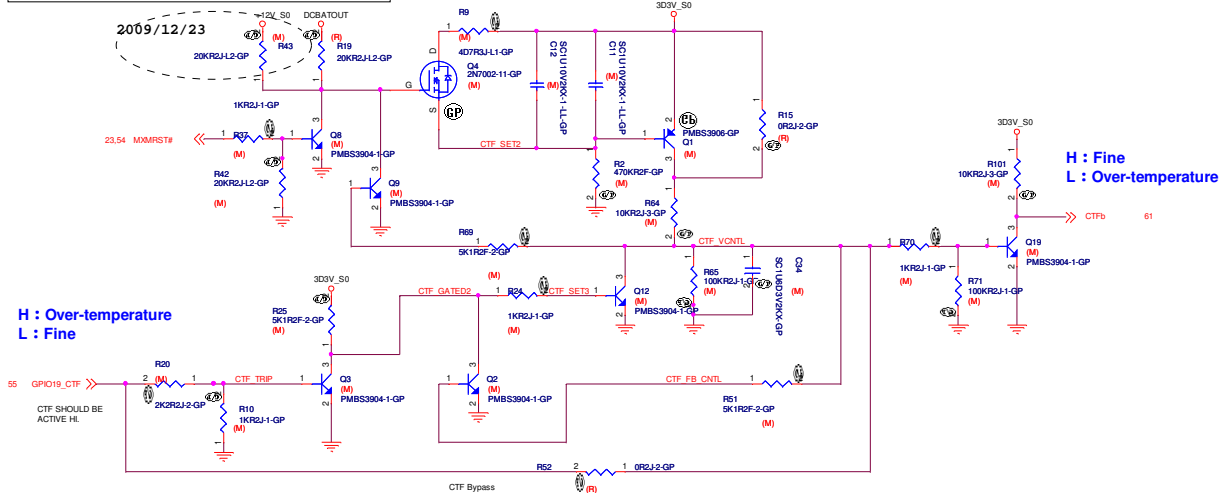
Title	<b>GPU PWR Sequence</b>
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Size	Document Number	Rev
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	<b>B305</b>	<b>1E</b>
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Critical Temperature Fault
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DIS / UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title **CTF/PPLAY**

Size C	Document Number <b>B305</b>	Rev <b>1B</b>
Date: Saturday, April 24, 2010	Sheet 62 of 62	